19-3479; Rev 0; 10/04

EVALUATION KIT AVAILABLE

EEPROM-Programmable, Quad, Power-Supply Tracker/Sequencer Circuit

General Description

The MAX6876 EEPROM-configurable, multivoltage power tracker/supervisor monitors four system voltages and ensures proper power-up and power-down conditions for systems requiring voltage tracking and/or sequencing. The MAX6876 provides a highly configurable solution as key thresholds and timing parameters are programmed through an I²C* interface and these values are stored in internal EEPROM. The MAX6876 also provides supervisory functions and an overcurrent detection circuit.

The MAX6876 features programmable undervoltage and overvoltage thresholds for each input supply. When all voltages are within specifications, the device turns on the external n-channel MOSFETs to either sequence or track the voltages to the system. All of the voltages can be sequenced or tracked or powered up with a combination of the two options. During tracking, the voltage at the GATE of each MOSFET is increased to slowly turn on each supply. The voltages at the source of each MOSFET are compared to each other to ensure that the voltage differential between each monitored supply does not exceed 250mV (typ). Tracking is dynamically adjusted to force all outputs to track within a ±125mV window from a reference ramp; if, for any reason, any supply fails to track within ±250mV from the reference ramp, a $\overline{\text{FAULT}}$ output is asserted, the power-up mode is terminated, and all outputs are powered off. Power-up mode is also terminated if the controlled voltages fail to complete the ramp-up within a programmable $\overline{\text{FAULT}}$ timeout. The MAX6876 features latch-off and autoretry modes to power on again after a fault condition has been detected.

Other features of the MAX6876 include a reset circuit, a manual reset input ($\overline{\text{MR}}$), and a margin disable input ($\overline{\text{MARGIN}}$). The device also features outputs for indicating a power-good condition (PG_) and an overcurrent condition ($\overline{\text{OC}}$), and a bus-removal (REM) output.

The MAX6876 is available in a small 6mm x 6mm, 36-pin thin QFN package and is fully specified over the extended -40°C to +85°C temperature range.

Applications

Multivoltage Systems
Networking Systems
Telecom
Storage Equipment
Servers/Workstations

**Purchase of I²C components from Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.*

SMBus is a trademark of Intel Corp.

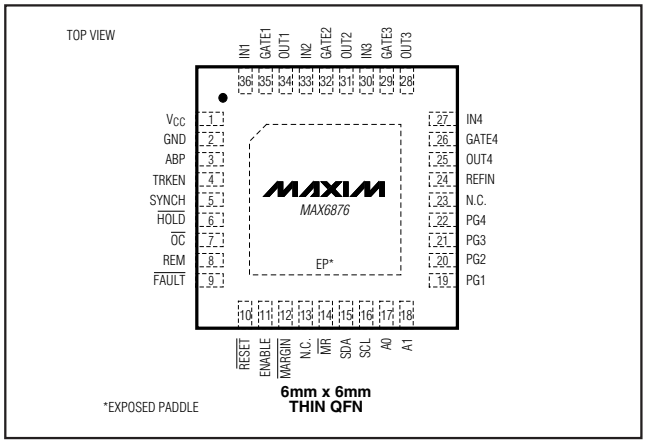
Features

- **Tracking/Sequencing for Up to Four Supply Voltages (With One MAX6876 Device) and Tracking for Up to 16 Supply Voltages (Using Four MAX6876 Devices)**
- **EEPROM-Configurable Tracking/Sequencing Control**
- **Bus Voltage Independent Operation (MAX6876 Is Powered from the Tracked Supply Voltages or Always-On Supply)**
- **EEPROM-Selectable Undervoltage/Overvoltage-Lockout Thresholds for Each Input Supply**
- **EEPROM-Selectable Power-Up/Down Slew Rate**
- **Programmable Power-Good Output Thresholds and Timing**
- **Global Adjustable Undervoltage Lockout or Logic ENABLE Input**
- **Independent Internal Charge Pumps to Enhance External n-Channel FETs (V_{GATE_SOURCE} = 5V)**
- **Post Power-Up Selectable Overcurrent Detection**
- **0.5V to 5.5V IN_ Threshold Range**
- **±1.5% Threshold Accuracy**
- **I²C/SMBus™-Compatible Serial Interface**
- **Small 6mm x 6mm, 36-Pin Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6876ETX	-40°C to +85°C	36 Thin QFN	T3666-3

Pin Configuration



EEPROM-Programmable, Quad, Power-Supply Tracker/Sequencer Circuit

ABSOLUTE MAXIMUM RATINGS

(All voltages are referenced to GND, unless otherwise noted.)
GATE_.....-0.3V to (IN_ + 6V)
IN1–IN4, V_{CC}.....-0.3V to +6V
OUT1–OUT4, SYNCH, ABP, REFIN.....-0.3V to Max (IN1–IN4, V_{CC}) + 0.3V
$\overline{ENABLE}$, TRKEN, $\overline{HOLD}$, $\overline{FAULT}$, $\overline{MR}$, $\overline{MARGIN}$.....-0.3V to +6V
$\overline{RESET}$, PG1–PG4, $\overline{OC}$, REM.....-0.3V to +6V
SDA, SCL, A0, A1.....-0.3V to +6V
Input/Output Current (all pins except OUT_ and GND) ...±20mA
OUT_, GND Current.....±50mA
Continuous Power Dissipation (T_A = +70°C)
36-Pin, 6mm x 6mm Thin QFN
(derate 26.3mW/°C above +70°C).....2105mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC}, IN1–IN4 = +2.7V to +5.5V; ENABLE = $\overline{MARGIN}$ = $\overline{MR}$ = ABP = TRKEN; T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 2)	V_{CC}	GATE_ = PG_ = $\overline{RESET}$ = 0		1.4			V
		Voltage on ABP (from V_{CC} or IN1–IN4) to ensure the device is fully operational		2.7		5.5	
Undervoltage Lockout	V_{UVLO}	Minimum voltage on ABP (from V_{CC} or IN1–IN4) to ensure the device is EEPROM configured				2.5	V
Supply Current	I_{CC}	V_{CC} = 5.5V, IN1–IN4 = 3.3V, no load			1.8	3	mA
		Configuration registers or memory access, no load			2.5	4	
IN_ Threshold Range	V_{TH}	IN1–IN4 (in 20mV increments)		1.00		5.50	V
		IN1–IN4 (in 10mV increments)		0.50		3.05	
Threshold Accuracy		T_A = 0°C to +85°C	0.5V < IN_ < 5.5V, IN_ falling for UV, rising for OV	-1.5		+1.5	%
		T_A = -40°C to +85°C	2V < IN_ < 5.5V, IN_ falling for UV, rising for OV (20mV increments)	-2.5		+2.5	%
			1V < IN_ < 2V, IN_ falling for UV, rising for OV (20mV increments)	-50		+50	mV
			1V < IN_ < 3.05V, IN_ falling for UV, rising for OV (10mV increments)	-2.5		+2.5	%
			0.5V < IN_ < 1V, IN_ falling for UV, rising for OV (10mV increments)	-25		+25	mV
Threshold Hysteresis	V_{TH_HYS}				0.5		$\%V_{TH}$
$\overline{RESET}$ Threshold Tempco	$\Delta V_{TH/C}$				50		ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC}, IN1–IN4 = +2.7V to +5.5V; ENABLE = $\overline{MARGIN}$ = $\overline{MR}$ = ABP = TRKEN; T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Tracking-Differential-Voltage Hold Ramp (Note 3)	V_{TRK}	$V_{OUT\_} > V_{TH\_PL}$ $V_{OUT\_} < V_{TH\_PG}$			95	125	155	mV
Tracking-Differential-Voltage Hysteresis						25		mV
Tracking-Differential $\overline{FAULT}$ Voltage (Note 3)	V_{TRK_F}	$V_{OUT\_} > V_{TH\_PL}$ $V_{OUT\_} < V_{TH\_PG}$			200	250	300	mV
$\overline{FAULT}$ Timeout Period (Note 4)	$t_{FAULTUP}$, $t_{FAULTDOWN}$	Register contents (Table 16)	00		20	25	30	ms
			01		40	50	60	
			10		80	100	120	
			11		160	200	240	
$\overline{FAULT}$ to GATE Delay	t_{FG}					2		µs
IN1–IN4 Input Impedance	R_{IN1-4}	For IN_ voltages < the highest IN_ supply			55	90	145	kΩ
OUT1–OUT4 Input Impedance	R_{OUT1-4}	OUT_ pulldown disabled			70	100	130	kΩ
Power-On Delay	t_{PO}	$V_{ABP} \geq V_{UVLO}$					3	ms
IN_ to GATE_ Delay	t_{D-GATE}	IN_ falling/rising, 100mV overdrive				6		µs
OUT_ to PG_ Delay	t_{POK}	OUT_ rising, 100mV overdrive				3		ms
		OUT_ falling, 100mV overdrive				25		µs
GATE, $\overline{RESET}$, Autoretry Timeout Period (Notes 5, 6)	t_{RESET}, t_{AUTO}, t_{GATE}	Register contents (Table 16)	000			25		µs
			001		10	12.5	15	ms
			010		20	25	30	
			011		40	50	60	
			100		80	100	120	
			101		160	200	240	
			110		320	400	480	
			111		1280	1600	1920	
$\overline{OC}$ Timeout Period	t_{OC}	Register contents (Table 16)	00		10	12.5	15	ms
			01		40	50	60	
			10		80	100	120	
			11		160	200	240	
Track/Sequence Slew Rate Rising or Falling	TRK_{SLEW}	Register contents (Table 16)	00	T_A = 0°C to +85°C	560	800	1040	V/s
				T_A = -40°C to 0°C	480	800	1120	
			01	T_A = 0°C to +85°C	280	400	520	
				T_A = -40°C to 0°C	240	400	560	
			10	T_A = 0°C to +85°C	140	200	260	
				T_A = -40°C to 0°C	120	200	280	
			11	T_A = 0°C to +85°C	70	100	130	
				T_A = -40°C to 0°C	60	100	140	
IN_ to OUT_ Overcurrent Threshold	V_{TH_OC}	Register contents (Table 16), OUT_ falling	00		96.25	97.5	98.75	%
			01		93.75	95	96.25	
			10		91.25	92.5	93.75	
			11		88.75	90	91.25	

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC}, IN1–IN4 = +2.7V to +5.5V; ENABLE = $\overline{MARGIN}$ = $\overline{MR}$ = ABP = TRKEN; T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN_ to OUT_ Power-Good Threshold	V_{TH_PG}	Register contents (Table 16), OUT_ rising	00	93.75	95	96.25	%
			01	91.25	92.5	93.75	
			10	88.75	90	91.25	
			11	86.25	87.5	88.75	
V_{TH_PG} and V_{TH_OC} Hysteresis	V_{OUT_HYS}				0.5		%
Power Low Threshold	V_{TH_PL}	OUT_ falling		125	142	165	mV
Power Low Hysteresis	$V_{TH\_PL\_HYS}$				10		mV
OUT_ to GND Pulldown Impedance (When Enabled)		ABP ≥ 2.5V			100		Ω
REM Output Low	V_{OL_REM}	ABP ≥ 2.5V, I_{SINK} = 4mA				0.3	V
		ABP ≥ 4.0V, I_{SINK} = 15mA				0.4	
Output Low PG1–PG4, $\overline{HOLD}$, $\overline{FAULT}$, $\overline{OC}$, $\overline{RESET}$ (Note 2)	V_{OL}	ABP ≥ 1.4V, I_{SINK} = 50µA (PG_, $\overline{RESET}$ only)				0.3	V
		ABP ≥ 2.5V, I_{SINK} = 1mA				0.3	
		ABP ≥ 4.0V, I_{SINK} = 4mA				0.4	
GATE1–GATE4 Output Low	V_{GOL}	ABP ≥ 1.4V, I_{SINK} = 50µA				0.3	V
		ABP ≥ 2.5V, I_{SINK} = 1mA				0.3	
		ABP ≥ 4.0V, I_{SINK} = 4mA				0.8	
PG1–PG4, $\overline{HOLD}$, $\overline{FAULT}$, $\overline{OC}$, $\overline{RESET}$, REM Output Open-Drain Leakage Current	I_{LKG}	Output deasserted		-1		+1	µA
GATE_ Output-Voltage High	V_{GOH}	$I_{GATE\_}$ = 0.5µA		IN_ + 4.4	IN_ + 5	IN_ + 5.8	V
GATE_ Pullup Current	I_{GATEUP}	During power-up/down, $V_{GATE\_}$ = 1V		2.5	4.5		µA
GATE_ Pulldown Current	$I_{GATEDOWN}$	During power-up/down, $V_{GATE\_}$ = 4V		2.5	4.5		µA
$\overline{MARGIN}$, $\overline{FAULT}$, $\overline{HOLD}$, $\overline{MR}$, ENABLE Input Voltage	V_{IL}					0.3 x ABP	V
	V_{IH}			0.6 x ABP			
$\overline{MR}$ Input Pulse Width	t_{MR}			2			µs
$\overline{FAULT}$, $\overline{HOLD}$, $\overline{MARGIN}$, $\overline{MR}$, ENABLE Glitch Rejection					100		ns
Digital Input to Logic Delay, $\overline{FAULT}$, $\overline{HOLD}$, $\overline{MARGIN}$, $\overline{MR}$, ENABLE	t_D				1		µs
$\overline{MARGIN}$, $\overline{MR}$ Digital Input to ABP Pullup Resistance	R_P			70	100	130	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC}, IN1–IN4 = +2.7V to +5.5V; ENABLE = $\overline{MARGIN}$ = $\overline{MR}$ = ABP = TRKEN; T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRKEN Input Delay	t_{EN}	TRKEN falling, 100mV overdrive		2		µs
TRKEN Reference Voltage Range	V_{TRKEN}	Input rising	1.245	1.285	1.320	V
		Input falling	1.225	1.25	1.275	
TRKEN Input Current	I_{TRKEN}	V_{TRKEN} = 1.25V	-100		+100	nA
Reference Input Voltage Range	V_{REFIN}		1.225	1.25	1.275	V
Reference Input Resistance	R_{REFIN}	V_{REFIN} = 1.25V		500		kΩ
SERIAL INTERFACE LOGIC (SDA, SCL, A0, A1)						
Logic-Input Low Voltage	V_{IL}				0.3 x ABP	V
Logic-Input High Voltage	V_{IH}		0.6 x ABP			V
Input Leakage Current	I_{ILKG}				1	µA
Output-Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
Output Leakage Current	I_{OLKG}				1	µA
Input/Output Capacitance	$C_{I/O}$			10		pF
SERIAL INTERFACE TIMING (SDA, SCL)						
Serial Clock Frequency	f_{SCL}				400	kHz
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Bus Free Time	t_{BUF}		1.3			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low to Valid Output	t_{AA}		0.1		0.9	µs
Data Out Hold Time	t_{DH}		50			ns
Data In Setup Time	$t_{SU:DAT}$		100			ns
Data In Hold Time	$t_{HD:DAT}$		0			ns
SCL/SDA Rise Time	t_R			300		ns
SCL/SDA Fall Time	t_F			300		ns
Transmit SDA Fall Time	t_F	C_{BUS} = 400pF	20 + 0.1 x C_{BUS}		300	ns
SCL/SDA Noise Suppression Time	t_I			50		ns
Byte Write Cycle Time	t_{WR}				11	ms

Note 1: Specifications guaranteed for the stated global conditions. 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.

Note 2: The internal supply voltage, measurable on ABP, is equal to the maximum of IN1–IN4 and V_{CC} supplies.

Note 3: Differential between each of the OUT_ and the SYNCH ramp voltage during power-up/down measured as $V_{OUT\_}$ - 2 x V_{SYNCH}.

Note 4: $\overline{FAULT}$ timeout starts to count at the beginning of each sequence of power-up/down and clears when the programmed OUT_ voltages track successfully.

EEPROM-Programmable, Quad, Power-Supply Tracker/Sequencer Circuit

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC}, IN1–IN4 = +2.7V to +5.5V; ENABLE = $\overline{MARGIN}$ = $\overline{MR}$ = ABP = TRKEN; T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

Note 5: The MAX6876 programmed as a single device; GATE timeout has counted prior to beginning each sequence of power-up. GATE timeout is not enabled during power-down or when the device is programmed as a master/slave.

Note 6: The MAX6876 programmed as a single device, the autoretry time begins to count at the assertion of the $\overline{FAULT}$ signal. The MAX6876 programmed as a master/slave device; the autoretry time begins to count at the deassertion of the common $\overline{FAULT}$ signal.

Timing Diagrams

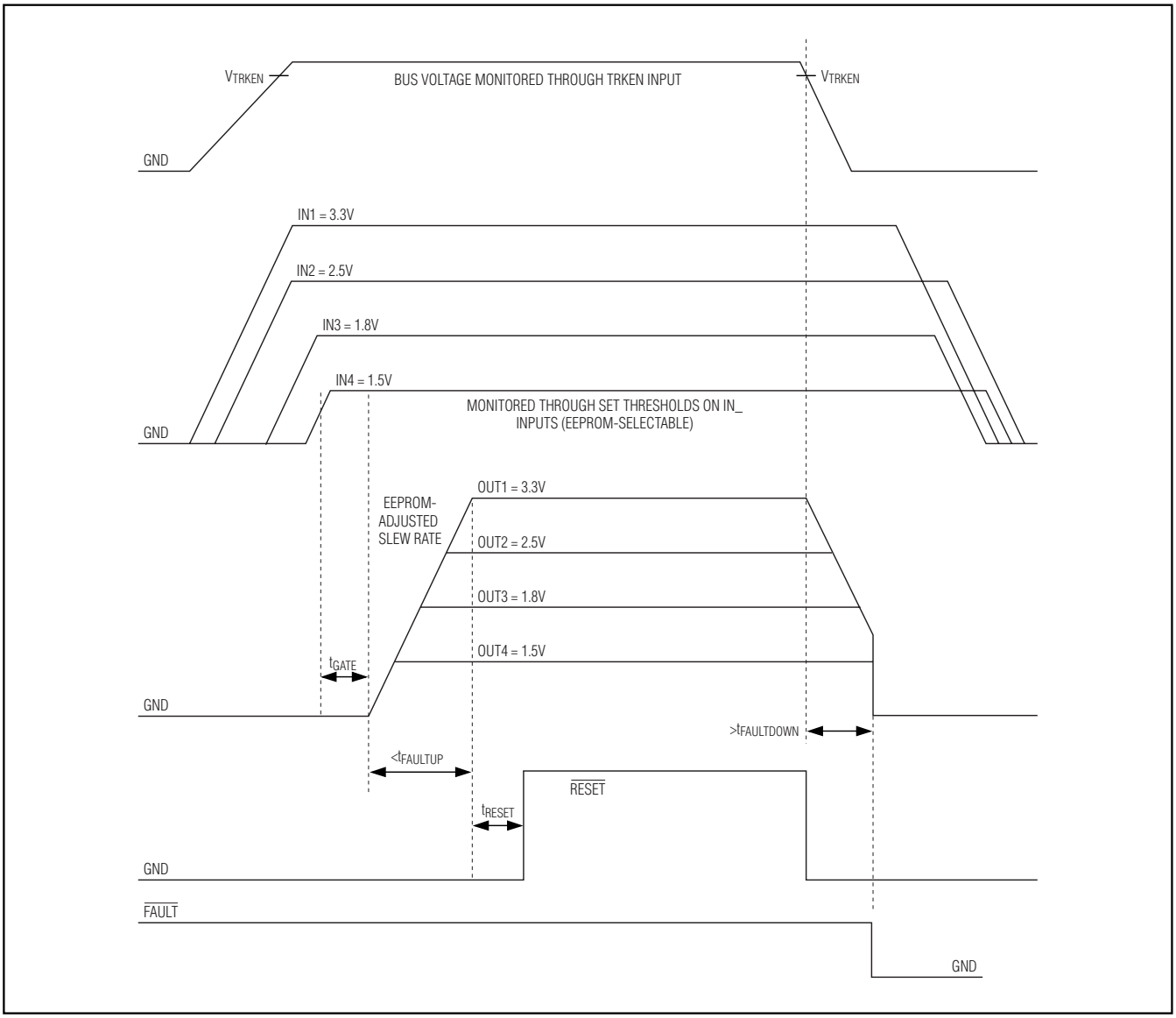


Figure 1. Tracking Timing Diagram

Timing Diagrams (continued)

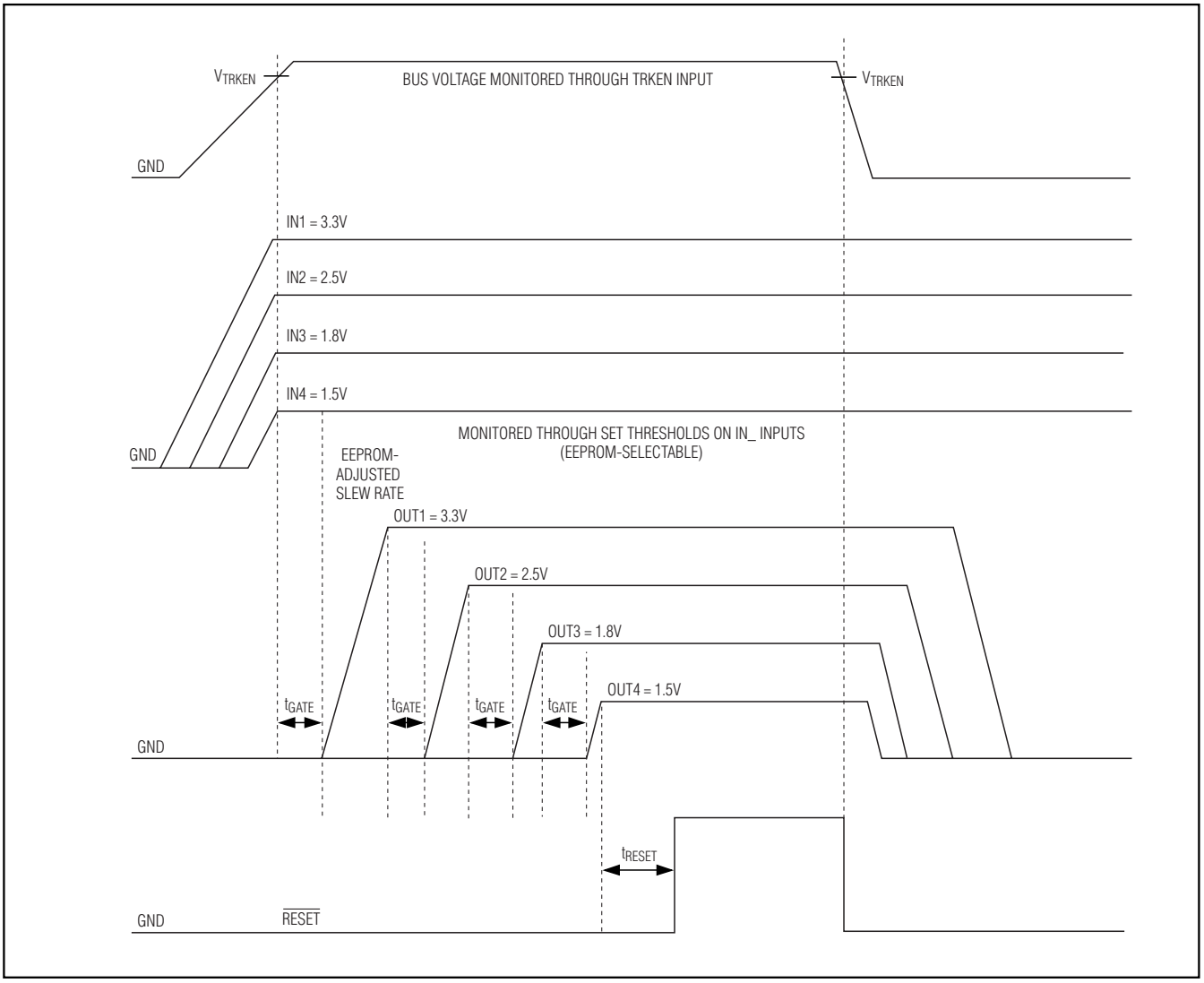


Figure 2. Sequencing Timing Diagram

EEPROM-Programmable, Quad, Power-Supply Tracker/Sequencer Circuit

Timing Diagrams (continued)

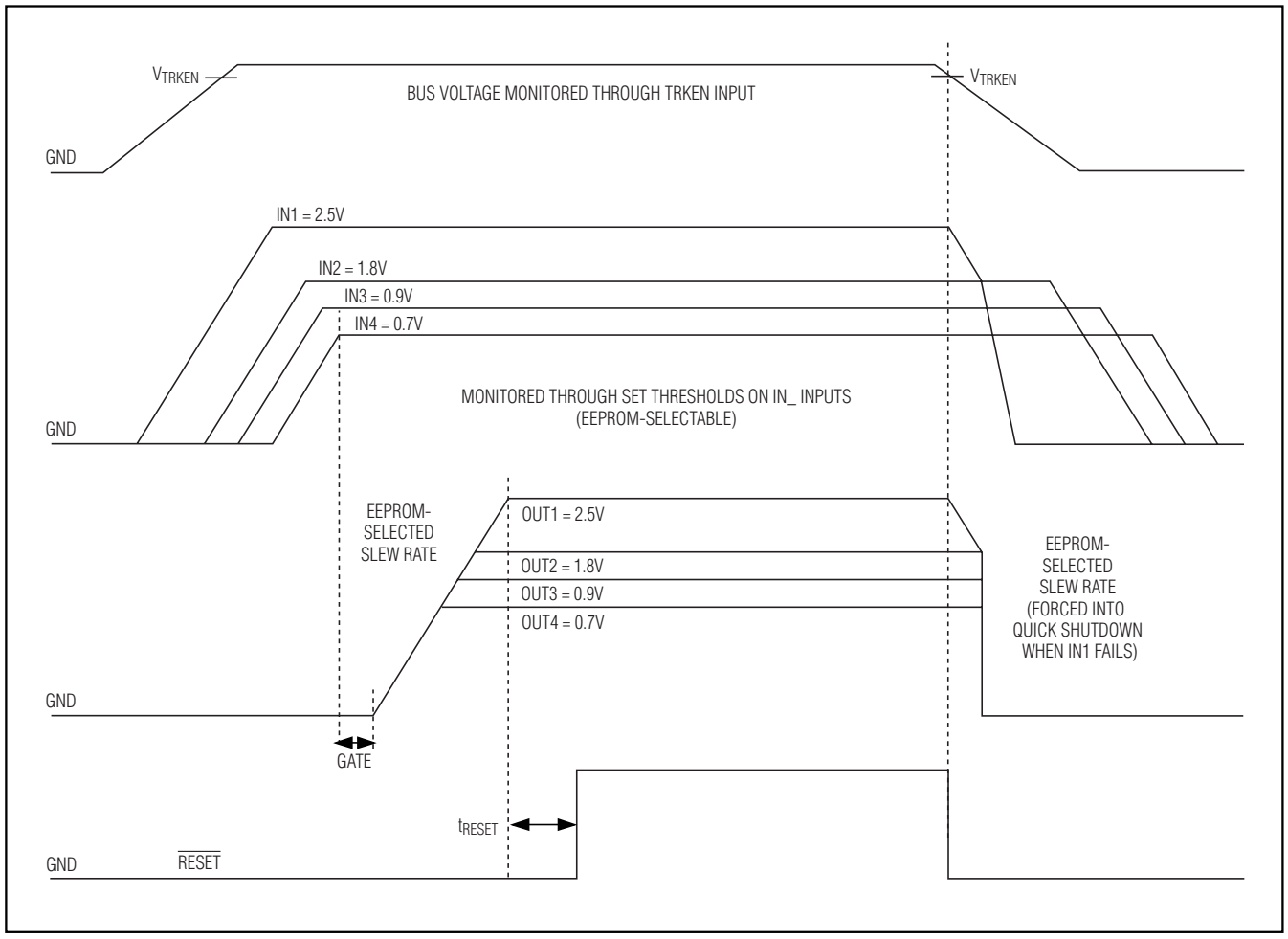


Figure 3. Voltage Tracking with Forced Shutdown (IN1 UV Failure)

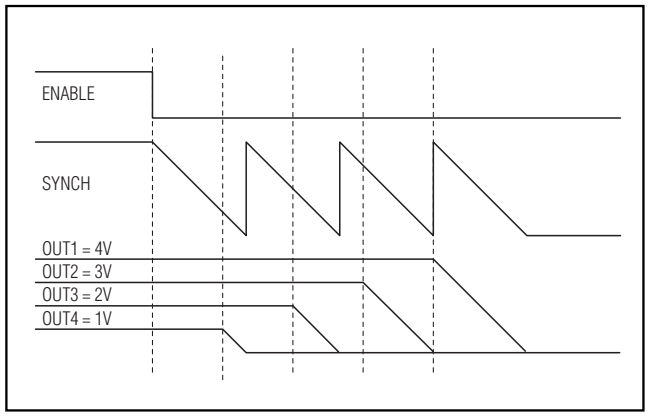


Figure 4. Sequencing Ramp Down Diagram

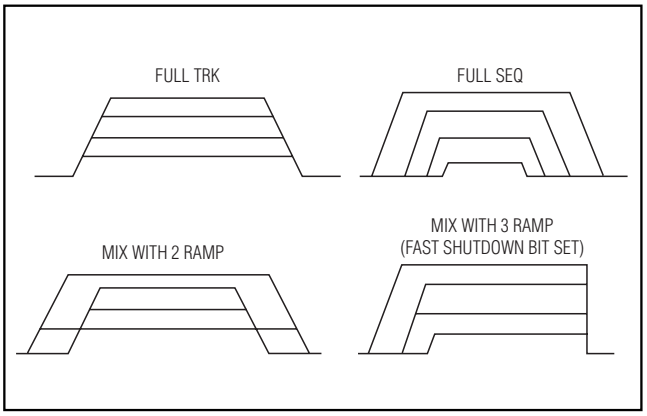


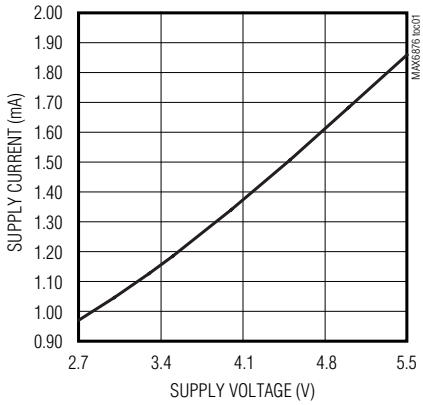
Figure 5. Mixed-Mode Tracking/Sequencing Examples

EEPROM-Programmable, Quad, Power-Supply Tracker/Sequencer Circuit

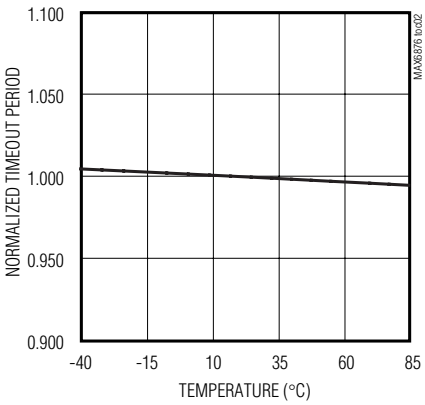
Typical Operating Characteristics

(V_{CC} = 3.3V, ENABLE = $\overline{MARGIN}$ = $\overline{MR}$ = ABP = TRKEN, T_A = +25°C, unless otherwise noted.)

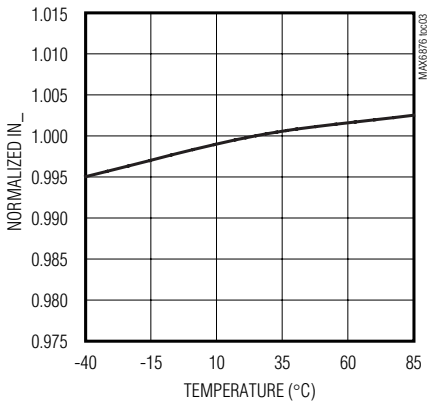
SUPPLY CURRENT vs. SUPPLY VOLTAGE



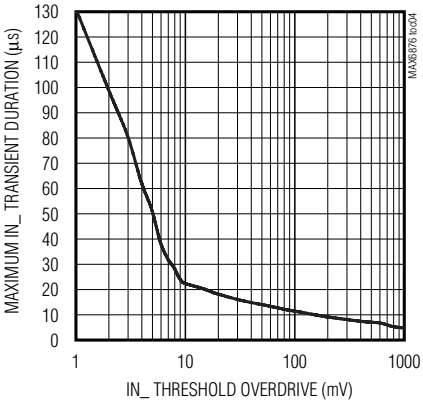
NORMALIZED TIMEOUT PERIOD vs. TEMPERATURE



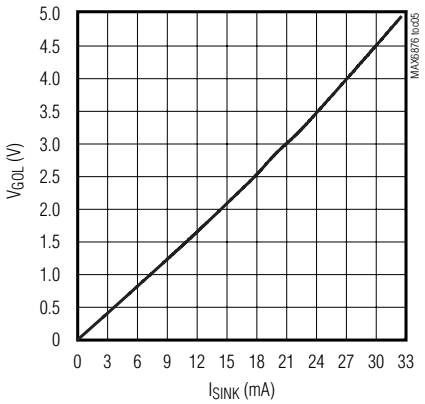
NORMALIZED IN_ THRESHOLD vs. TEMPERATURE



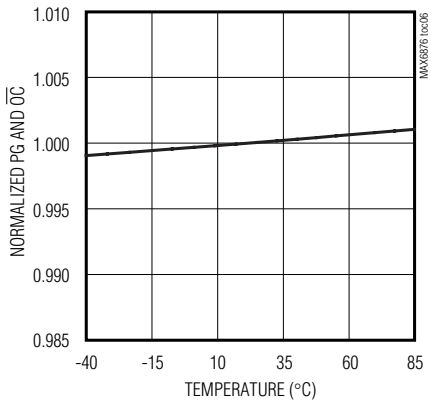
MAXIMUM IN_ TRANSIENT DURATION vs. IN_ THRESHOLD OVERDRIVE



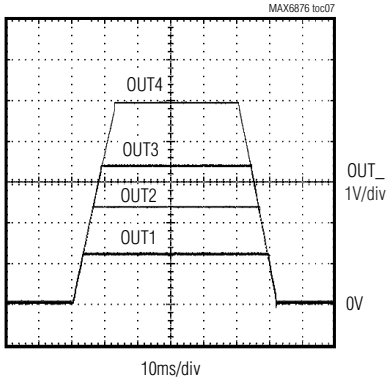
GATE OUTPUT-VOLTAGE LOW vs. SINK CURRENT



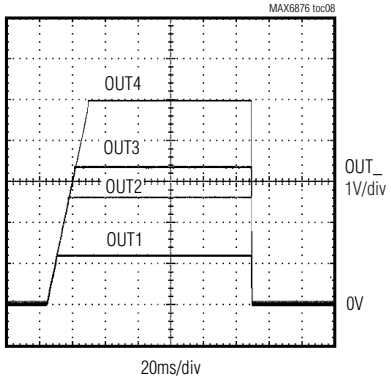
NORMALIZED PG AND $\overline{OC}$ THRESHOLD vs. TEMPERATURE



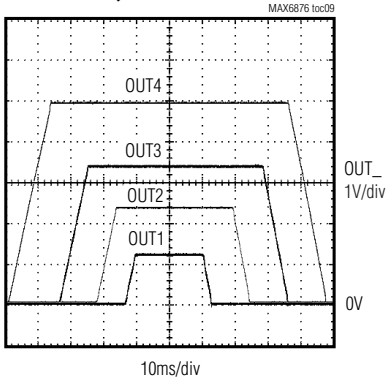
TRACKING MODE



TRACKING MODE WITH FAST SHUTDOWN



SEQUENCING MODE

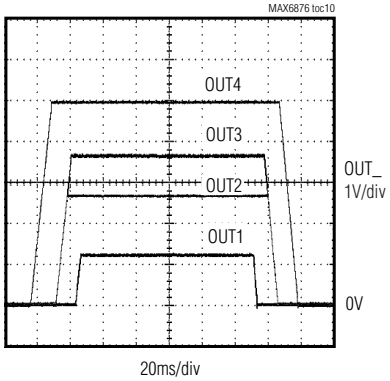


EEPROM-Programmable, Quad, Power-Supply Tracker/Sequencer Circuit

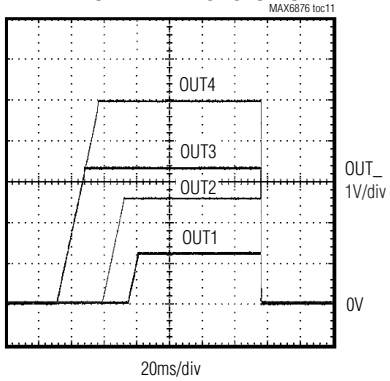
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, ENABLE = $\overline{MARGIN}$ = $\overline{MR}$ = ABP = TRKEN, T_A = +25°C, unless otherwise noted.)

MIXED MODE



MIXED MODE WITH FAST SHUTDOWN



Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Optional Supply Voltage Input. Connect V_{CC} to an alternate (i.e., always-on) supply if desired. V_{CC} supports operation/communication when the monitored supplies are not powered or are below the minimum required operating voltage. In a master/slave application, connect all V_{CC} pins to a common supply line.
2	GND	Ground
3	ABP	Internal Analog Bypass. Bypass ABP with a 1µF capacitor to GND. ABP maintains the device supply voltage during rapid power-down conditions.
4	TRKEN	Tracking Enable Input. TRKEN must be higher than 1.285V to enable voltage tracking power-up operation. When TRKEN falls below 1.25V (3% hysteresis), OUT_ tracks down. Connect TRKEN to an external resistor-divider network to set the desired monitor threshold. Connect TRKEN to ABP if not used.
5	SYNCH	Selectable Tracking Synchronization Output/Input. SYNCH allows multiple MAX6876 devices to control tracking of multiple power supplies (up to 16 voltages on the same I^2C bus). One device is programmed as SYNCH master and all other devices are programmed as slaves. SYNCH on the master outputs the common ramp voltage to which all OUT_ voltages are tracked (with active control loops). SYNCH of the slave devices is input for the ramp control voltage (no internal ramp is generated in the slaves) (see the *SYNCH* section). Connect SYNCH to other SYNCH pins only.
6	$\overline{HOLD}$	Active-Low, Open-Drain Synchronization Hold Output/Input. $\overline{HOLD}$ communicates synchronization status between master/slave devices in multiple MAX6876 applications. The $\overline{HOLD}$ output remains asserted while selected tracking IN_ inputs are below their selected thresholds (the slave device can delay tracking start until its inputs are at their required stable voltage levels) or held low by the master when it is counting the autoretry time after a detected fault condition (see the *Synchronization Hold Output ($\overline{HOLD}$)* section). Slave device SYNCH are inputs for the ramp control voltage.

Pin Description (continued)

PIN	NAME	FUNCTION
7	$\overline{OC}$	Active-Low, Open-Drain Overcurrent Output. $\overline{OC}$ asserts low if any monitored IN_ to OUT_ voltage falls out of the selected percentage of the IN_ voltage range (V_{TH_OC}) for more than the programmed t_{OC}. $\overline{OC}$ monitoring begins only after supply tracking or sequencing has been completed and is disabled during power-down operation.
8	REM	Open-Drain Bus Removal Output. REM signals when it is safe to remove the card after a controlled track/sequence-down operation. REM goes high impedance when all $V_{OUT\_} < V_{TH\_PL}$. REM requires an external pullup resistor. In master/slave mode, REM can be ORed together (the common REM connection remains low if any $V_{OUT\_} > V_{TH\_PL}$ threshold) *(*see the *Typical Application Circuit* and the *Bus Removal Output (REM)* section).
9	$\overline{FAULT}$	Active-Low, Open-Drain Tracking Fault Alert Output or Input. $\overline{FAULT}$ asserts low if a tracking failure is present for longer than the specified fault period or if tracking voltages fails by more than ±250mV (see the *$\overline{FAULT}$* section).
10	$\overline{RESET}$	Active-Low, Open-Drain Reset or Power-Good Output. $\overline{RESET}$ is low during power-up and power-down tracking. $\overline{RESET}$ goes high after all selected OUT_ outputs exceed their selected thresholds and the reset timeout period t_{RESET} has expired. The reset timeout period is internally selectable. $\overline{RESET}$ requires an external pullup resistor.
11	ENABLE	Logic ENABLE Input. ENABLE must be high to enable voltage tracking/sequencing power-up operation. OUT_ begins tracking down when ENABLE is low. Connect to ABP if not used.
12	$\overline{MARGIN}$	Active-Low Margin Input. The $\overline{MARGIN}$ function allows systems to be tested with supply voltages outside their normal ranges without affecting supply tracking/sequencing or reset states. $\overline{MARGIN}$ functionality is usually enabled after systems have powered up in normal mode. The $\overline{MARGIN}$ functionality is disabled (returns to normal monitoring mode) after $\overline{MARGIN}$ returns high. $\overline{MARGIN}$ is internally pulled up to ABP through a 100kΩ resistor.
13, 23	N.C.	No Connection. Not internally connected.
14	$\overline{MR}$	Active-Low Manual Reset Input. When $\overline{MR}$ is low, $\overline{RESET}$ goes low and remains asserted for the selected timeout period after $\overline{MR}$ is pulled high. $\overline{MR}$ is internally pulled up to ABP through a 100kΩ resistor.
15	SDA	Serial-Interface Data Input/Output (Open-Drain). SDA requires an external pullup resistor.
16	SCL	Serial-Interface Clock Input. SCL requires an external pullup resistor.
17	A0	Serial-Interface Address Inputs. The inputs allow up to four MAX6876 devices to be addressed when sharing a common data bus. A1 and A0 should be connected to GND or ABP.
18	A1	
19	PG1	Power-Good Output, Open-Drain. Each PG_ output signals when its monitored OUT_ voltage is within the selected percentage of the IN_ voltage range (V_{TH_PG}). PG_ is low until OUT_ exceeds the programmable threshold (V_{TH_PG}) for more than t_{POK}. PG_ outputs are open-drain and require external pullups if used.
20	PG2	
21	PG3	
22	PG4	

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Pin Description (continued)

PIN	NAME	FUNCTION
24	REFIN	Reference Voltage Input. The MAX6876 can be configured to use the internal 1.25V reference or an external voltage reference. REFIN is tri-stated when using the internal reference. REFIN provides the threshold voltage for the voltage detectors when using an external voltage reference. Use an external voltage reference when tighter voltage-detector accuracy is desired. When configured to an internal reference, leave REFIN unconnected. When configured for an external reference, connect a 1.225V to 1.275V reference to REFIN.
25	OUT4	Monitored Output Voltage. The OUT4 output is monitored to control the supply slew rate and tracking performance. OUT1–OUT4 begin to track up after the internal supply (ABP) exceeds the minimum voltage requirements, V_{TRKEN} > 1.285V threshold, ENABLE is logic high, and IN1–IN4 are all within their selected thresholds. The OUT4 output falls out of the tracking equation as OUT4 approaches IN4; other OUT_ supplies continue tracking up without signaling a system fault. OUT_ outputs are tracked down during power-off conditions.
26	GATE4	Gate Drive for External n-Channel FETs. GATE4 begins enhancing the external n-channel FETs when all monitored inputs are within their selected thresholds (0.5V to 5.5V), at least one IN_ input or V_{CC} is above the minimum operating voltage, V_{TRKEN} > 1.285V threshold, and the ENABLE input is logic high. During power-up mode, GATE_ voltages are enhanced with internal control loops forcing all OUT_ voltages to track the reference ramp (SYNCH) at a programmed slew rate. An internal charge pump boosts GATE4 to V_{IN4} + 5V to fully enhance the external n-channel FET when power-up is complete.
27	IN4	Supply Voltage and Tracked Input Voltage. Nominal supply range is 0.5V to 5V. IN1, IN2, IN3, IN4, or V_{CC} must be greater than the internal UVLO (V_{ABP} = 2.7V) to enable the tracking functionality. The IN4 input is monitored with internally selected thresholds to ensure all supplies have stabilized before tracking (or sequencing) is enabled.
28	OUT3	Monitored Output Voltage. OUT3 is monitored to control the supply slew rate and tracking performance. OUT1–OUT4 begin to track up after the internal supply (ABP) exceeds the minimum voltage requirements, V_{TRKEN} > 1.285V threshold, ENABLE is logic high, and IN1–IN4 are all within their selected thresholds. The OUT3 output falls out of the tracking equation as OUT3 approaches IN3; other OUT_ supplies continue tracking up without signaling a system fault. OUT_ outputs are tracked down during power-off conditions.
29	GATE3	Gate Drive for External n-Channel FETs. GATE3 begins enhancing the external n-channel FETs when all monitored inputs are within their selected thresholds (0.5V to 5.5V), at least one IN_ input or V_{CC} is above the minimum operating voltage, V_{TRKEN} > 1.285V threshold, and the ENABLE input is logic high. During power-up mode, GATE_ voltages are enhanced with internal control loops forcing all OUT_ voltages to track the reference ramp (SYNCH) at a programmed slew rate. An internal charge pump boosts GATE3 to V_{IN3} + 5V to fully enhance the external n-channel FET when power-up is complete.
30	IN3	Supply Voltage and Tracked Input Voltage. Nominal supply range is 0.5V to 5V. IN1, IN2, IN3, IN4, or V_{CC} must be greater than the internal UVLO (V_{ABP} = 2.7V) to enable the tracking functionality. IN3 is monitored with internally selected thresholds to ensure all supplies have stabilized before tracking (or sequencing) is enabled.
31	OUT2	Monitored Output Voltage. OUT2 is monitored to control the supply slew rate and tracking performance. OUT1–OUT4 begin to track up after the internal supply (ABP) exceeds the minimum voltage requirements, V_{TRKEN} > 1.285V threshold, ENABLE is logic high, and IN1–IN4 are all within their selected thresholds. OUT2 output falls out of the tracking equation as OUT2 approaches IN2; other OUT_ supplies continue tracking up without signaling a system fault. OUT_ outputs are tracked down during power-off conditions.

Pin Description (continued)

PIN	NAME	FUNCTION
32	GATE2	Gate Drive for External n-Channel FETs. GATE2 begins enhancing the external n-channel FETs when all monitored inputs are within their selected thresholds (0.5V to 5.5V), at least one IN_ input or V_{CC} is above the minimum operating voltage, V_{TRKEN} > 1.285V threshold, and the ENABLE input is logic high. During power-up mode, GATE_ voltages are enhanced with internal control loops forcing all OUT_ voltages to track the reference ramp (SYNCH) at a programmed slew rate. An internal charge pump boosts GATE2 to V_{IN2} + 5V to fully enhance the external n-channel FET when power-up is complete.
33	IN2	Supply Voltage and Tracked Input Voltage. Nominal supply range is 0.5V to 5V. IN1, IN2, IN3, IN4, or V_{CC} must be greater than the internal UVLO (V_{ABP} = 2.7V) to enable the tracking functionality. IN2 is monitored with internally selected thresholds to ensure all supplies have stabilized before tracking (or sequencing) is enabled.
34	OUT1	Monitored Output Voltage. Each OUT1 is monitored to control the supply slew rate and tracking performance. OUT1–OUT4 begin to track up after the internal supply (ABP) exceeds the minimum voltage requirements, V_{TRKEN} > 1.285V threshold, ENABLE is logic high, and IN1–IN4 are all within their selected thresholds. The OUT1 output falls out of the tracking equation as OUT1 approaches IN1; other OUT_ supplies continue tracking up without signaling a system fault. OUT_ outputs are tracked down during power-off conditions.
35	GATE1	Gate Drive for External n-Channel FETs. GATE1 begins enhancing the external n-channel FETs when all monitored inputs are within their selected thresholds (0.5V to 5.5V), at least one IN_ input or V_{CC} is above the minimum operating voltage, V_{TRKEN} > 1.285V threshold, and the ENABLE input is logic high. During power-up mode, GATE_ voltages are enhanced with internal control loops forcing all OUT_ voltages to track the reference ramp (SYNCH) at a programmed slew rate. An internal charge pump boosts GATE1 to V_{IN1} + 5V to fully enhance the external n-channel FET when power-up is complete.
36	IN1	Supply Voltage and Tracked Input Voltage. Nominal supply range is 0.5V to 5V. IN1, IN2, IN3, IN4, or V_{CC} must be greater than the internal UVLO (V_{ABP} = 2.7V) to enable the tracking functionality. IN1 is monitored with internally selected thresholds to ensure all supplies have stabilized before tracking (or sequencing) is enabled.
—	EP	Exposed Paddle. Exposed paddle is internally connected to GND.

Detailed Description

The MAX6876 EEPROM-configurable, multivoltage power tracker/supervisor monitors four system voltages and ensures proper power-up and power-down conditions for systems requiring voltage tracking and/or sequencing. The MAX6876 provides a highly configurable solution as key thresholds and timing parameters are programmed through an I²C interface and these values are stored in internal EEPROM. In addition to tracking and sequencing voltages, the MAX6876 also provides supervisory functions as well as an overcurrent detection circuit.

The MAX6876 features programmable undervoltage and overvoltage thresholds for each input supply. The thresholds are EEPROM configured in 10mV (0.5V to 3.05V) or 20mV (1.0V to 5.5V) increments. When all of the voltages are within their specifications, the device turns on the external n-channel MOSFETs to either sequence or track the voltages to the system. All of the voltages can be sequenced or tracked or powered up with a combination of the two options. During voltage tracking, the voltage at the GATE of each MOSFET is increased to slowly turn on each OUT_. The GATE delay is EEPROM-selectable from 25µs to 1.6s. The

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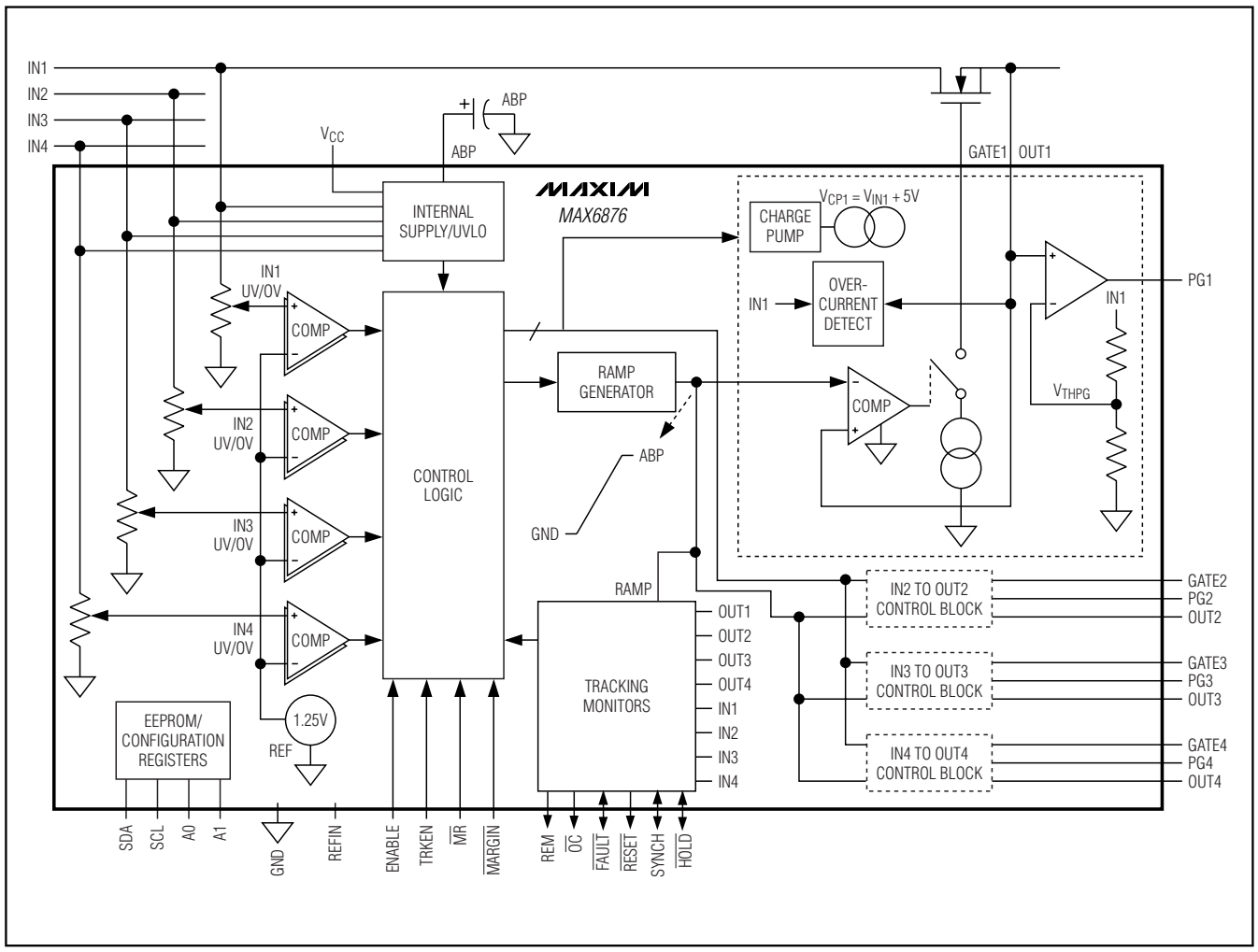
Functional Diagram



voltages at the sources of the MOSFETs are compared to each other to ensure that the voltage differential between each monitored supply does not exceed 250mV (typ). Tracking is dynamically adjusted to force all outputs to track within a ±125mV window from a reference ramp; if, for any reason, any supply fails to track within ±250mV from the reference ramp, the FAULT output is asserted, the power-up mode is terminated, and all outputs are powered off. Power-up mode is in the same way terminated if the controlled voltages fail to complete the ramp up within a programmable FAULT timeout. The MAX6876 generates all required voltages (with internal charge pumps) and timing to control up to four external n-channel MOSFETs for the OUT1–OUT4 supply voltages.

A synchronization feature allows up to 16 voltages to be tracked simultaneously. In addition, HOLD and SYNCH communicate synchronization status between master/slave devices in multiple MAX6876 applications.

Other features of the MAX6876 include a reset circuit with an I²C-programmable timeout feature. A manual reset input (MR) and a margin disable input (MARGIN) allow for more control during the manufacturing process. The device also features four power-good outputs (PG_), an overcurrent output (OC), and a bus-removal safe (REM) output. The device has an accurate internal 1.25V reference; for greater accuracy, connect an external +1.25V reference to REFIN.

Table 1. Master/Slave Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
09h	29h	[7:6]	If "00," the device configuration is a single device.
			If "01," the device configuration is multiple devices, slave.
			If "10," the device configuration is multiple devices, slave.
			If "11," the device configuration is multiple devices, master.

Modes of Operation

The MAX6876 provides three different modes of operation: tracking, sequencing, and mixed modes. The mixed mode is a combination of both tracking and sequencing modes (see the *Mixed Mode (Tracking/Sequencing)* section).

Tracking

When all selected inputs exceed their selected thresholds, V_{TRKEN} > 1.285V, and ENABLE is logic high, the tracking process is initialized. The MAX6876 generates an internal ramp voltage that drives the control loops for the desired tracked voltage. The tracking functionality is monitored with a comparator control block (see the *Functional Diagram* and Figure 5). The comparators monitor and control each output voltage with respect to the common tracking ramp voltage to stay within a ±125mV differential window, monitor each tracked output voltage with respect to its input voltage, and monitor each output voltage with respect to GND during power-up/retry cycles. Under normal conditions each OUT_ voltage will track the ramp voltage until the OUT_ voltage approximates the IN_ voltage (the external n-channel FET is saturated). The slew rate for the ramp voltage is selected through EEPROM.

Master/Slave Operation (Tracking Only)

To support voltage tracking for more than four supplies, combine multiple MAX6876 devices. Two MAX6876 devices (one master/one slave) track up to eight supply voltages and four MAX6876 devices (one master and three slaves) track up to 16 supply voltages. Each device must be programmed to act in master or slave mode (only one master is allowed); the default state is single device (see Table 1). The MAX6876 outputs the ramp control voltage with the SYNCH output when configured as a master device. This ramp allows multiple devices to synchronize with the master when slave SYNCHs are configured as inputs. For proper functionality control, connect all ENABLE pins together. In master/slave mode, all controlled supplies are tracked up/down (no mixed sequencing/tracking modes are supported). In master-slave application, the part is intended to provide only tracking for the four supplies (only one ramp is generated). To control one particular channel, insert a "1" in any of the four possible positions (one row for each channel contains 4 bits) and the circuit will generate the proper signals (see Figure 6).

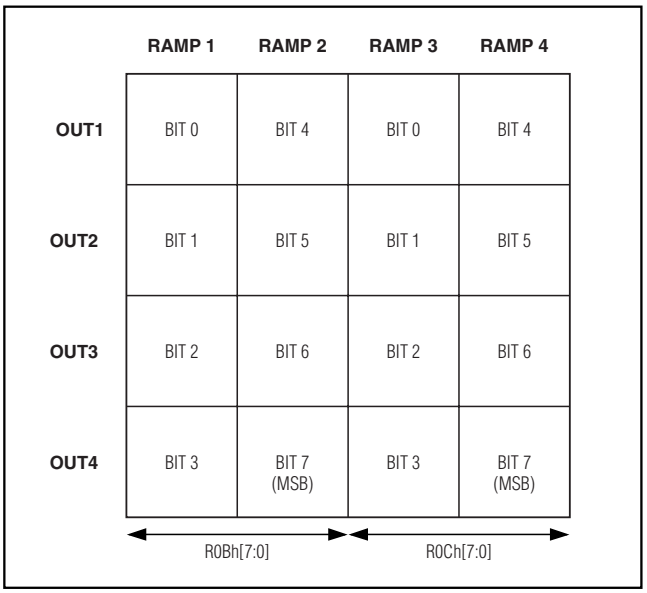


Figure 6. Mapping Tracking and Sequencing Modes

For multiple MAX6876 operations, the ramp control voltage is brought out of the master's SYNCH (programmed as an output) and into the slave's SYNCH (programmed as an input). The highest tracked supply must be connected to one of the master's IN_ inputs. When all IN_ threshold conditions are met (on master and slaves), the master ramp begins rising at the selected ramp slew rate. During normal operation all OUT_ voltages (for master and slave) track the ramp voltage. If the slave's OUT_ voltages do not properly follow the ramp voltage (exceed 125mV differential), the slave device asserts $\overline{HOLD}$ low. The master recognizes the $\overline{HOLD}$ and holds the ramp voltage, allowing the slave's slower OUT_ voltages to

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catch up. When the slave's voltages approach the ramp voltage, the slave releases HOLD and the master allows the ramp voltage to begin rising again. All tracking must be completed by the selected tracking fault timeout period or the supplies are powered down. The slave HOLD output is asserted low until the selected tracking IN_ voltages are within their selected thresholds. This ensures that the master does not begin the tracking operation until the slave's input voltages (IN_) have properly stabilized.

Sequencing

The sequencing operation can be initialized by properly setting the bit of registers 0Bh and 0Ch. During a sequencing power-up phase, each OUT_ is independently powered on with a controlled slew rate. No more than one supply is powered on for each generated ramp. The bits of registers 0Bh and 0Ch establish the turn-on order. During each phase, the ramp is enabled to start only after the t_{GATE} timeout has been counted. The sequencing phase will be considered complete when all the channels programmed to power on reach the independently set PG_ thresholds (see Figure 5).

Mixed Mode (Tracking/Sequencing)

The MAX6876 is fully programmable to generate up to four ramps during power-up or power-down modes. Each OUT_ voltage independently is programmed to follow any of the control ramps generated by the MAX6876. To do the latter, set the bits on register 0Bh and 0Ch to "1" for each channel. The following are programming examples of different power-up modes (→ = sequence, / = track):

0Bh = 0000 1111 0Ch = 0000 0000 tracking mode: OUT1/OUT2/OUT3/OUT4 on Ramp1

0Bh = 1000 0100 0Ch = 0010 0001 sequencing mode: OUT3 → OUT4 → OUT1 → OUT2 on Ramp1, Ramp2, Ramp3, Ramp4

0Bh = 1100 0001 0Ch = 0010 0000 mix mode*: OUT1 → OUT4/OUT3 → OUT2 on Ramp1, Ramp2, Ramp4

*(Ramp3 is not considered because no OUT_ outputs are selected by bit [0:3] of 0Ch.)

Drive ENABLE or TRKEN low or use a software command to initiate a controlled power-down. The MAX6876 powers down the OUT_ voltages in a reverse sequence from the one at power-up when this option is selected.

For example, with the following power-up sequence:
OUT1 → OUT4/OUT3 → OUT2

then the power-down sequence will be:
OUT2 → OUT4/OUT3 → OUT1

Configuring Tracking and Sequencing Modes

To configure tracking and sequencing modes, insert "1" and "0" into the 0Bh and 0Ch registers (see Table 2). Figure 6 shows how to map for tracking and sequencing modes. Each OUT_ output can follow one of the four possible ramps in tracking or sequencing mode (16 bits are available) and one bit set to "1," means that the channel of the interested row is powered up/down by the corresponding ramp (see Figure 6).

1) If the depicted table (in Figure 6) is made by all "1s," the part simply generates a single ramp (all channels in tracking mode since the first column is full of "1s,") and it ignores the remaining values of the other 12 bits.
2) If one row contains more than one symbol "1," only the first encountered (columns starting with R0Bh [3:0]) is taken into account and the channel is powered up/down with the corresponding ramp.
3) If there is one (or more) row in which all 4 bits are set to "0," it means that the device will not control that particular channel.
4) If there is one (or more) column where all 4 bits are set to "0," the device skips that ramp and its associate $t_{D\text{-}GATE}$.

In master-slave applications, the device is intended to provide only tracking for the four supplies (only one ramp can be generated). To control one particular channel, only insert a "1" in any of the four possible positions (one row for each channel contains 4 bits) and the device generates the proper signals. When three or less ramps are needed, use consecutive ramps starting with ramp 1.

Power-Down and Power-Up

When all the IN_ inputs are within the selected threshold range and the internal enable is logic high (Figure 7), the device initiates a power-up phase. During power-up, the OUT_ outputs are forced by an internal loop that controls the GATE_ of the external MOSFET to follow the reference ramp voltage. This phase for each individual ramp must be completed within the programmable fault timeout time; otherwise, the part will force a shutdown on the GATE_. Once the power-up is completed, a power-down phase can be initiated by forcing the internal enable low. Two power-down options are available: a fast-shutdown option where all GATE_ gates are quickly turned off or a reverse-order option. This reverse-order option allows the OUT_ voltage to be powered down with a controlled slew rate and in the reverse order they have been powered up (see Figure 2).

Table 2. Configuring Tracking and Sequencing Modes

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
0Bh	2Bh	[7:0]	Bit 7—If 1, OUT4 on ramp 2
			Bit 6—If 1, OUT3 on ramp 2
			Bit 5—If 1, OUT2 on ramp 2
			Bit 4—If 1, OUT1 on ramp 2
			Bit 3—If 1, OUT4 on ramp 1
			Bit 2—If 1, OUT3 on ramp 1
			Bit 1—If 1, OUT2 on ramp 1
			Bit 0—If 1, OUT1 on ramp 1
0Ch	2Ch	[7:0]	Bit 7—If 1, OUT4 on ramp 4
			Bit 6—If 1, OUT3 on ramp 4
			Bit 5—If 1, OUT2 on ramp 4
			Bit 4—If 1, OUT1 on ramp 4
			Bit 3—If 1, OUT4 on ramp 3
			Bit 2—If 1, OUT3 on ramp 3
			Bit 1—If 1, OUT2 on ramp 3
			Bit 0—If 1, OUT1 on ramp 3

To speed up the discharge of the OUT_ voltage, an optional 100Ω pulldown resistor can be selected (see Table 3).

Slew-Rate Control

The reference ramp voltage slew rate during any controlled power-up/down phase can be programmed in the 100V/s to 800V/s range. Before any power-up or retry cycle, the MAX6876 must first ensure that all OUT_ voltages are near ground (below the V_{TH_PL} power low threshold). An internal programmable tracking timeout period can be selected to signal a fault and shut down the output voltages if tracking takes too long (see Table 4).

Power-supply tracking operation should be completed within the selected fault timeout period. For selected control ramps of 100V/s the normal tracking time should be approximately 50ms (5V supply, SR = 100V/s). The total tracking time is extended when the MAX6876 must vary the control slew rate to allow slow supplies to catch up. If the external FET is too small (RDS is too high for the selected load current and IN_ source current), the OUT_ voltage may never reach the control ramp voltage.

Autoretry and Latch-Off Functions

The MAX6876 features latch-off or autoretry mode to power on again after a fault condition has been detected. Toggle ENABLE, I^2C command bit, and TRKEN or cycle device power to clear the latch. Set bit 5 of register 09h to "1" to program the MAX6876 in latch-off mode, or "0" to program for autoretry mode. The autoretry time can be programmed with bits 2, 3, and 4 of register 09h (see Table 5). During autoretry, the gate drive remains off and $\overline{FAULT}$ remains asserted. In a master-slave application, $\overline{FAULT}$ is asserted low until all the OUT_ outputs of each device are discharged to GND, and only the master counts the autoretry time while $\overline{HOLD}$ remains low (see Table 5).

Stability Comment

No external compensation is required for tracking or slew-rate control.

Powering the MAX6876

The MAX6876 derives power from V_{CC} or the voltage-detector inputs: IN1–IN4 (see the *Functional Diagram*). V_{CC} (if being used) or one of the IN_ inputs must be at least +2.7V to ensure full device operation.

The highest input voltage on IN1–IN4 or V_{CC} supplies power to the device. Internal hysteresis ensures that the supply input that initially powers the device continues to power the device when multiple input voltages are within 50mV (typ) of each other.

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Table 3. Program Power-Down and Power-Up

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
13h	33h	[7:3]	Bit 7—If 1, reverse order of track/sequence power-down If 0, GATE_ fast pulldown
			Bit 6—If 1, OUT1 charges with internal pulldown If 0, no pulldown is allowed
			Bit 5—If 1, OUT2 charges with internal pulldown If 0, no pulldown is allowed
			Bit 4—If 1, OUT3 charges with internal pulldown If 0, no pulldown is allowed
			Bit 3—If 1, OUT4 charges with internal pulldown If 0, no pulldown is allowed
0Ah	2Ah	[7:6]	"00" fault power-up timer value = 25ms
			"01" fault power-up timer value = 50ms
			"10" fault power-up timer value = 100ms
			"11" fault power-up timer value = 200ms
		[5:4]	"00" fault power-down timer value = 25ms
			"01" fault power-down timer value = 50ms
			"10" fault power-down timer value = 100ms
			"11" fault power-down timer value = 200ms

Table 4. Setting the Slew Rate

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
12h	32h	Bit [7:6]	"00" track/sequence slew rate (rise or fall) = 800V/s
			"01" track/sequence slew rate (rise or fall) = 400V/s
			"10" track/sequence slew rate (rise or fall) = 200V/s
			"11" track/sequence slew rate (rise or fall) = 100V/s

Inputs

IN1–IN4

The IN1–IN4 voltage detectors monitor voltages from 1V to 5.5V in 20mV increments, or +0.5V to +3.05V in 10mV increments. Use the following equations to set the threshold voltages for IN_:

$$x = \frac{V_{TH} - 1V}{0.02V}$$

for +1V to +5.5V range.

$$x = \frac{V_{TH} - 0.5V}{0.01V}$$

for +0.5V to +3.05V range.

where V_{TH} is the desired threshold voltage and x is the decimal code for the desired threshold (Table 6). For the +1V to +5.5V range, x must equal 225 or less; otherwise, the threshold exceeds the maximum operating voltage of IN1–IN4 (Table 6). An overvoltage or undervoltage failure on an IN_ input immediately shuts down all the OUT_ outputs and generates a $\overline{FAULT}$ in the master/slave condition.

Table 5. Program Autoretry/Latch off

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
09h	29h	5	If 1, latch-on fault If 0, autoretry
		[4:2]	“000” autoretry timer value = 25µs
			“001” autoretry timer value = 12.5ms
			“010” autoretry timer value = 25.0ms
			“011” autoretry timer value = 50.0ms
			“100” autoretry timer value = 100.0ms
			“101” autoretry timer value = 200.0ms
			“110” autoretry timer value = 400.0ms
			“111” autoretry timer value = 1600.0ms

Table 6. IN1–IN4 Threshold Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
00h	20h	[7:0]	IN1 Undervoltage Threshold V_{TH} = 1.0 + n x 20mV (if R08[7] = 0) V_{TH} = 0.5 + n x 10mV (if R08[7] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
01h	21h	[7:0]	IN2 Undervoltage Threshold V_{TH} = 1.0 + n x 20mV (if R08[6] = 0) V_{TH} = 0.5 + n x 10mV (if R08[6] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
02h	22h	[7:0]	IN3 Undervoltage Threshold V_{TH} = 1.0 + n x 20mV (if R08[5] = 0) V_{TH} = 0.5 + n x 10mV (if R08[5] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
03h	23h	[7:0]	IN4 Undervoltage Threshold V_{TH} = 1.0 + n x 20mV (if R08[4] = 0) V_{TH} = 0.5 + n x 10mV (if R08[4] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
04h	24h	[7:0]	IN1 Overvoltage Threshold V_{TH} = 1.0 + n x 20mV (if R08[7] = 0) V_{TH} = 0.5 + n x 10mV (if R08[7] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.

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Table 6. IN1–IN4 Threshold Settings (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
05h	25h	[7:0]	IN2 Overvoltage Threshold V_{TH} = 1.0 + n x 20mV (if R08[6] = 0) V_{TH} = 0.5 + n x 10mV (if R08[6] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
06h	26h	[7:0]	IN3 Overvoltage Threshold V_{TH} = 1.0 + n x 20mV (if R08[5] = 0) V_{TH} = 0.5 + n x 10mV (if R08[5] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
07h	27h	[7:0]	IN4 Overvoltage Threshold V_{TH} = 1.0 + n x 20mV (if R08[4] = 0) V_{TH} = 0.5 + n x 10mV (if R08[4] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
08h	28h	[7:4]	Bit 7—If 0, 20mV steps in V_{TH} setting for IN1 If 1, 10mV steps in V_{TH} setting for IN1
			Bit 6—If 0, 20mV steps in V_{TH} setting for IN2 If 1, 10mV steps in V_{TH} setting for IN2
			Bit 5—If 0, 20mV steps in V_{TH} setting for IN3 If 1, 10mV steps in V_{TH} setting for IN3
			Bit 4—If 0, 20mV steps in V_{TH} setting for IN4 If 1, 10mV steps in V_{TH} setting for IN4

Manual Reset Input ($\overline{MR}$)

The manual reset ($\overline{MR}$) input initiates a reset condition. $\overline{MR}$ is internally pulled up to ABP through a 100kΩ resistor. When $\overline{MR}$ is low, $\overline{RESET}$ remains low for the selected reset timeout period after $\overline{MR}$ transitions from low to high (see the *Reset Output ($\overline{RESET}$)* section).

Margin Input ($\overline{MARGIN}$)

$\overline{MARGIN}$ allows system-level testing while power supplies exceed the normal ranges. Drive $\overline{MARGIN}$ low before varying system voltages below/above the selected threshold without signaling an error. $\overline{MARGIN}$ makes it possible to vary the supplies without a need to reprogram the IN_ or PG_ thresholds and prevents tracker/sequencer alerts or faults. Drive $\overline{MARGIN}$ high or leave it floating for normal operating mode.

ENABLE

Drive logic ENABLE input high to initiate voltage tracking/sequencing during power-up operation. Drive logic ENABLE low to initiate tracking/sequencing power-down operation. When ENABLE is not used, connect to ABP.

When the MAX6876 is configured to use the I²C on/off command, a valid I²C signal must be received before the device begins the power-up tracking/sequencing routine. The internal enable logic is an AND function of the ENABLE logic, the TRKEN logic, and the I²C control/command logic (Figure 7). When all three AND gate input variables are true (and the monitored IN/OUT voltages meet their required thresholds), turn-on is allowed. When any AND input variable becomes false, the turn-off cycle (track/sequence down) begins immediately. Drive ENABLE and TRKEN high if only the I²C command is to be used to turn on/off the device. The detectors monitoring IN_ and OUT_ voltages, and overcurrent conditions have a higher priority after a power-on routine has been initiated by the internal enable logic. If a fault occurs during the power-up cycle, the device is powered down immediately, independent of ENABLE, TRKEN, and the I²C shutdown

Table 7. Program ENABLE

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
09h	29h	[1:0]	Bit 1—If 1, check ENABLE with I²C enable control bit If 0, ignore ENABLE with I²C
			Bit 0—If 0, enable with I²C = 0, I²C enable command bit If 1, enable with I²C = 1

Table 8. Select External Reference

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
11h	31h	0	Bit 0—If 1, selects external reference; 0 selects internal reference

command (Table 7). If a latch-on fault mode is chosen, a toggle on the internal enable clears the latch condition and restarts the device after a fault condition (Figure 7).

Reference Voltage Input (REFIN)

The MAX6876 features an internal +1.25V voltage reference. The voltage reference sets the threshold of the voltage detectors. Leave REFIN unconnected when using the internal reference. REFIN accepts an external reference in the +1.225V to +1.275V range. Use Table 8 commands to select the external reference.

Track Enable Input (TRKEN)

The track enable (TRKEN) monitor input is another feature of the MAX6876. To enable voltage-tracking power-up operation, drive TRKEN higher than 1.285V. When TRKEN goes below 1.25V, OUT_ outputs start tracking down. Connect TRKEN to an external resistor-divider network to set the desired monitor threshold. Connect TRKEN to ABP if not used.

SYNCH

The MAX6876 provides selectable tracking synchronization output or input (SYNCH). SYNCH allows tracking of up to 16 power supplies on the same I²C bus. One device is programmed as the SYNCH master and the other devices are programmed as slaves. SYNCH of the master device outputs the common ramp voltage to which all OUT_ voltages are tracked. The SYNCH pins of the slave devices are inputs for the ramp control voltage (no internal ramp is generated in the slave devices) (see Table 1).

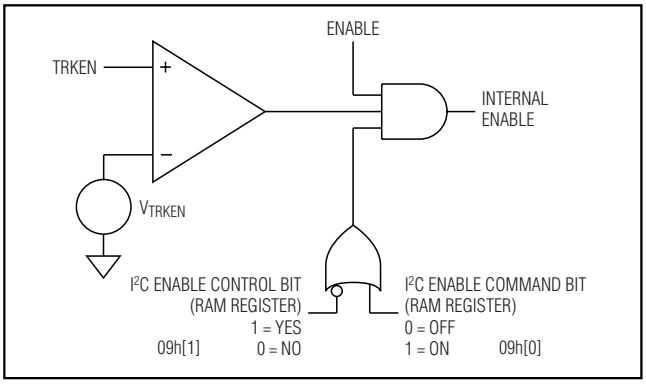

Figure 7. Logic ENABLE

Monitored Outputs

OUT1–OUT4

The MAX6876 monitors four OUT_ outputs to control the tracking/sequencing performance. After the internal supply (ABP) exceeds the minimum voltage (2.7V) requirements, TRKEN > 1.25V, the internal ENABLE input is logic high, and IN1–IN4 are all within their selected thresholds, OUT1–OUT4 will begin to track or sequence.

During power-up mode, the MAX6876 drives the gates of the external n-channel FETs to force the OUT_ voltages to track the internally set ramp voltage. If OUT_ voltages vary from the ramp voltage by more than ±125mV, an internal comparator signals an alert that dynamically adjusts the ramp voltage (stops the ramp until the slow OUT_ catches up). During power-down mode, an internal pulldown resistor (100Ω) on OUT_ can be enabled to help discharge load capacitance.

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Table 9. GATE-Delay Time Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
0Fh	2Fh	[7:5]	"000" gate-delay timer value = 25µs
			"001" gate-delay timer value = 12.5ms
			"010" gate-delay timer value = 25.0ms
			"011" gate-delay timer value = 50.0ms
			"100" gate-delay timer value = 100.0ms
			"101" gate-delay timer value = 200.0ms
			"110" gate-delay timer value = 400.0ms
			"111" gate-delay timer value = 1600.0ms

Table 10. $\overline{\text{FAULT}}$ Power-Up and Power-Down Time Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
0Ah	2Ah	[7:6]	Bit [7:6] "00" fault power-up timer value = 25ms "01" fault power-up timer value = 50ms "10" fault power-up timer value = 100ms "11" fault power-up timer value = 200ms
		[5:4]	Bit [5:4] "00" fault power-down timer value = 25ms "01" fault power-down timer value = 50ms "10" fault power-down timer value = 100ms "11" fault power-down timer value = 200ms

Outputs

GATE_

The MAX6876 features four GATE_ outputs to drive four external n-channel FET gates. The following conditions must be met before GATE_ begins enhancing the external n-channel FET_:

1) All monitored inputs (IN1–IN4) are above their selected thresholds (0.5V to 5.5V)
2) At least one IN_ input or V_{CC} is above 2.7V
3) Drive ENABLE high
4) TRKEN > 1.25V

At power-up mode, GATE_ voltages are enhanced control loops so all OUT_ voltages track together at a user-selected slew rate. Each GATE_ is internally pulled up to 5V above its relative IN_ voltage to fully enhance the external n-channel FET when power-up is complete. In sequencing/tracking mode, a gate delay timeout is internally counted prior to the start of each control ramp (see Figures 1 and 2 and Table 9).

$\overline{\text{FAULT}}$

The MAX6876 offers an open-drain, active-low tracking fault alarm ($\overline{\text{FAULT}}$). $\overline{\text{FAULT}}$ asserts low when a power-up phase is not completed within the specified fault period or if tracking voltages fail by more than ±250mV. For multiple MAX6876 applications, $\overline{\text{FAULT}}$ is an input/output pin and communicates fault information between master/slave devices. Connect all $\overline{\text{FAULT}}$ pins in an ORed configuration to force simultaneous shutdown on all MAX6876s (Table 10.) See the *Typical Application Circuit*.

Power-Good Outputs (PG_)

The MAX6876 features four power-good (PG_) outputs. PG_ outputs are open-drain and require external pullups.

When the OUT_ output is within the selected percentage of the IN_ voltage range (V_{TH_PG}), the corresponding PG_ output goes high impedance. PG_ stays low until the OUT_ voltage exceeds the programmable V_{TH_PG} threshold for more than t_{POK} (Table 11).

Table 11. PG Threshold Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
10h	30h	[7:6]	"00" IN4 to OUT4 power-good threshold = 95%
			"01" IN4 to OUT4 power-good threshold = 92.5%
			"10" IN4 to OUT4 power-good threshold = 90%
			"11" IN4 to OUT4 power-good threshold = 87.5%
		[5:0]	"00" IN3 to OUT3 power-good threshold = 95%
			"01" IN3 to OUT3 power-good threshold = 92.5%
			"10" IN3 to OUT3 power-good threshold = 90%
			"11" IN3 to OUT3 power-good threshold = 87.5%
			"00" IN2 to OUT2 power-good threshold = 95%
			"01" IN2 to OUT2 power-good threshold = 92.5%
			"10" IN2 to OUT2 power-good threshold = 90%
			"11" IN2 to OUT2 power-good threshold = 87.5%
			"00" IN1 to OUT1 power-good threshold = 95%
			"01" IN1 to OUT1 power-good threshold = 92.5%
			"10" IN1 to OUT1 power-good threshold = 90%
			"11" IN1 to OUT1 power-good threshold = 87.5%

Bus Removal Output (REM)

The MAX6876 features an open-drain bus removal (REM) output. REM signals when it is safe to remove the card after a controlled track/sequence power-down operation. To initiate a power-down, drive ENABLE low or send an I^2C power-down command. REM monitors OUT_ and when any of the OUT_ voltages are above the V_{TH_PL} threshold, REM stays low. When all OUT_ outputs are below V_{TH_PL}, REM goes high impedance. Connect REM to an external pullup resistor/LED chain to visually signal when it is safe to remove a powered board from the bus.

In tracking mode when REM is used in master/slave operations, connect all REM pins together. The common REM connection remains low if any OUT_ supply is above the V_{TH_PL} threshold.

Overcurrent Output ($\overline{OC}$)

The open-drain, active-low $\overline{OC}$ output asserts low if an overcurrent condition is detected in any selected channel for longer than t_{OC}. Overcurrent conditions are determined as a differential voltage between IN_ and OUT_. $\overline{OC}$ monitoring begins only after supply tracking or sequencing has been completed and is disabled during power-down operation (Table 12).

Reset Output ($\overline{RESET}$)

The reset output, $\overline{RESET}$, is an open-drain output that monitors the selected OUT_ voltages. The selected OUT_ voltages must exceed their selected PG_ thresholds for the selected reset timeout period (t_{RP}) before $\overline{RESET}$ is deasserted. A manual reset input ($\overline{MR}$) can assert $\overline{RESET}$. $\overline{RESET}$ remains low while $\overline{MR}$ is low. $\overline{RESET}$ remains low for the selected reset timeout period (t_{RP}) after $\overline{MR}$ transitions from low to high (Table 13).

Synchronization Hold Output ($\overline{HOLD}$)

The MAX6876 features an open-drain, active-low synchronization alert output/input. $\overline{HOLD}$ communicates synchronization status between master/slave devices in multiple MAX6876 applications. When a slave device detects a tracking problem with respect to the master SYNCH signal, the slave asserts $\overline{HOLD}$ low. When tracking is back under control, the slave's $\overline{HOLD}$ is deasserted and goes high again. The $\overline{HOLD}$ output remains asserted while selected tracking IN_ inputs are below their selected thresholds (the slave device can delay a tracking start until its inputs are at their required stable voltage levels) or held low by the master when it is counting the autoretry time after a detected fault condition. Connect $\overline{HOLD}$ pins only to other MAX6876 $\overline{HOLD}$ pins.

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Table 12. $\overline{OC}$ Threshold Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
0Dh	2Dh	[7:6]	Bit [7:6] "00" IN4 to OUT4 overcurrent threshold = 97.5% "01" IN4 to OUT4 overcurrent threshold = 95% "10" IN4 to OUT4 overcurrent threshold = 92.5% "11" IN4 to OUT4 overcurrent threshold = 90%
		[5:0]	Bit [5:4] "00" IN3 to OUT3 overcurrent threshold = 97.5% "01" IN3 to OUT3 overcurrent threshold = 95% "10" IN3 to OUT3 overcurrent threshold = 92.5% "11" IN3 to OUT3 overcurrent threshold = 90%
			Bit [3:2] "00" IN2 to OUT2 overcurrent threshold = 97.5% "01" IN2 to OUT2 overcurrent threshold = 95% "10" IN2 to OUT2 overcurrent threshold = 92.5% "11" IN2 to OUT2 overcurrent threshold = 90%
			Bit [1:0] "00" IN1 to OUT1 overcurrent threshold = 97.5% "01" IN1 to OUT1 overcurrent threshold = 95% "10" IN1 to OUT1 overcurrent threshold = 92.5% "11" IN1 to OUT1 overcurrent threshold = 90%
0Eh	2Eh	[7:1]	Bit [7:6] "00" overcurrent timer value = 12.5ms "01" overcurrent timer value = 50ms "10" overcurrent timer value = 100ms "11" overcurrent timer value = 200ms
			Bit 5—If 1, overcurrent monitoring on OUT1 is enabled If 0, no overcurrent monitoring on OUT1
			Bit 4—If 1, overcurrent monitoring on OUT2 is enabled If 0, no overcurrent monitoring on channel 1
			Bit 3—If 1, overcurrent monitoring on OUT3 is enabled If 0, no overcurrent monitoring on OUT3
			Bit 2—If 1, overcurrent monitoring on OUT4 is enabled If 0, no overcurrent monitoring on OUT4

ABP

ABP powers the analog circuitry. Bypass ABP to GND with a 1µF ceramic capacitor installed as close to the device as possible. Do not use ABP to provide power to external circuitry.

Configuring the MAX6876

The MAX6876 factory-default configuration sets all registers to 00h. This device requires configuration before full power is applied to the system. To configure the MAX6876, first apply an input voltage greater than 2.7V to one of IN1–IN4 or V_{CC} (see the *Powering the MAX6876* section). Next, transmit data with the serial interface. Use the block write protocol to quickly configure the device. Write to the configuration registers first, to ensure the device is configured properly. After completing the setup procedure, use the read word protocol to read back the data from the configuration registers. Lastly, use the write word protocol to write this data to the EEPROM registers. After completing the EEPROM register configuration, apply full power to the system to begin normal operation. The nonvolatile EEPROM stores the latest configuration upon removal of power (Table 14).

Software Reboot

A command code of C4h initiates a software reboot. A software reboot allows the user to restore the EEPROM configuration to the volatile registers without cycling the power supplies.

Table 13. Program $\overline{\text{RESET}}$

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
11h	31h	[7:1]	Bit 7—If 1, OUT1 also controls $\overline{\text{RESET}}$ If 0, OUT1 does not control $\overline{\text{RESET}}$
			Bit 6—If 1, OUT2 also controls $\overline{\text{RESET}}$ If 0, OUT2 does not control $\overline{\text{RESET}}$
			Bit 5—If 1, OUT3 also controls $\overline{\text{RESET}}$ If 0, OUT3 does not control $\overline{\text{RESET}}$
			Bit 4—If 1, OUT4 also controls $\overline{\text{RESET}}$ If 0, OUT4 does not control $\overline{\text{RESET}}$
			Bit [3:1] “000” reset timer value = 25µs “001” reset timer value = 12.5ms “010” reset timer value = 25.0ms “011” reset timer value = 50.0ms “100” reset timer value = 100.0ms “101” reset timer value = 200.0ms “110” reset timer value = 400.0ms “111” reset timer value = 1600.0ms

SMBus/I²C-Compatible Serial Interface

The MAX6876 features an I²C/SMBus-compatible 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX6876 and the master device at clock rates up to 400kHz. Figure 10 shows the 2-wire interface timing diagram. The MAX6876 is transmit/receive slave-only, relying upon a master device to generate a clock signal. The master device (typically a microcontroller) initiates a data transfer on the bus and generates SCL to permit that transfer.

A master device communicates to the MAX6876 by transmitting the proper address followed by command and/or data words. Each transmit sequence is framed by a START (S) or REPEATED START (SR) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse.

SCL is a logic input, while SDA is an open-drain input/output. SCL and SDA both require external pullup resistors to generate the logic-high voltage. Use 4.7kΩ for most applications.

Bit Transfer

Each clock pulse transfers one data bit. The data on SDA must remain stable while SCL is high (Figure 11); otherwise, the MAX6876 registers a START or STOP condition (Figure 12) from the master. SDA and SCL idle high when the bus is not busy.

Start and Stop Conditions

Both SCL and SDA idle high when the bus is not busy. A master device signals the beginning of a transmission with a START (S) condition (Figure 8) by transitioning SDA from high to low while SCL is high. The master device issues a STOP (P) condition (Figure 8) by transitioning SDA from low to high while SCL is high. A STOP condition frees the bus for another transmission. The bus remains active if a REPEATED START condition is generated, such as in the block read protocol (see Figure 11).

Early STOP Conditions

The MAX6876 recognizes a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition. This condition is not a legal I²C format; at least one clock pulse must separate any START and STOP condition.

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Table 14. Registers Summary

REGISTERS	DESCRIPTIONS
Input Undervoltage Thresholds (Registers 00h to 03h)	Input undervoltage thresholds (0.5V to 3.04V in 10mV increments or 1.0V to 5.5V in 20mV increments). Each channel's range is selected with register 08h.
Input Overvoltage Thresholds (Registers 04h to 07h)	Input overvoltage thresholds (0.5V to 3.04V in 10mV increments or 1.0V to 5.5V in 20mV increments). Each channel's range is selected with register 08h.
Tracking/Sequencing Modes	Selects if outputs are to be sequenced or tracked. Sequencing/tracking modes are defined by 4 bits for each OUT voltage of register 0Bh and 0Ch (see the *Track/Sequence* section).
Tracking/Sequencing Power-Up/Down Slew Rate	Selectable output slew rate for power-up/down mode. Selected slew is overwritten during tracking faults. Power-up/down slew rate is selected by bit [6:7] of register 12h.
Power-Up Delay Period	Power-up sequencing delay. Selects delay time for sequencing each supply. Programmable delays are selected with bit [5:7] of register 0Fh.
Power-Down Sequence/Track Behavior	Selectable power-down operation. Chooses if output voltages should be brought down in the reverse sequence from power-up mode selections or if power supplies should be simultaneously fast powered down (selected with bit 7 register 13h).
OUT Pulldown Enable	Selects if OUT_ should be internally pulled to GND when in fast shutdown or tracking fault mode (selected with bit [6:3] register 13h).
Single/Multiple Device Application	Selects if the device will be used alone or in a master/slave application. If a single application, the device can be operated in mixed sequencing/tracking modes. If multi-device application, the device can be operated in tracking mode only (selected with bit [7:6] register 09h). 00: single device 11: master device 01 or 10: slave device
Overcurrent Threshold	Selects IN_-to-OUT_ threshold voltage for overcurrent monitoring for each channel (register 0Dh).
Power-Good Threshold	Selects IN_-to-OUT_ threshold voltage for power-good monitoring for each channel (register 10h).
Overcurrent Assert Select	Selects which overcurrent monitors will assert the OC output (selected by bit [5:2] of reg. 0Eh).
Overcurrent Filter Period	Selects the filter time for the overcurrent monitors. OC will not assert until the overcurrent condition has existed longer than the selected filter period (selected by bit [7:6] of reg. 0Eh).
Fault Timeout Period	Selects the timeout period for sequencing/tracking completion. If sequencing/tracking operation is not complete before the fault timeout period, a $\overline{\text{FAULT}}$ alert will be signaled and all supplies will be powered down (selected by bit [7:4] of reg. 0Ah).
Fault Behavior	Selects how the device should operate during faults. Options include latch-off after fault or autoretry after fault. Autoretry delay is selectable (selected by bit 5 of reg. 09h).
Reset Assert Select	Selects which OUT detectors will assert the $\overline{\text{RESET}}$ output (selected by bit [7:4] of reg. 11h).
Reset Timeout Period Select	Selects the reset timeout period (selected by bit [3:1] of reg. 11h).
Enable the Part with I^2C Interface	Bit 0 and bit 1 of register 09h allows a micro to turn the MAX6876 on/off with the I^2C interface. While 09h[1] is 0, the part will ignore any enable command from I^2C. If 09h[1] is set to 1, then 09h[0] has to be 1 to enable the part to power on.

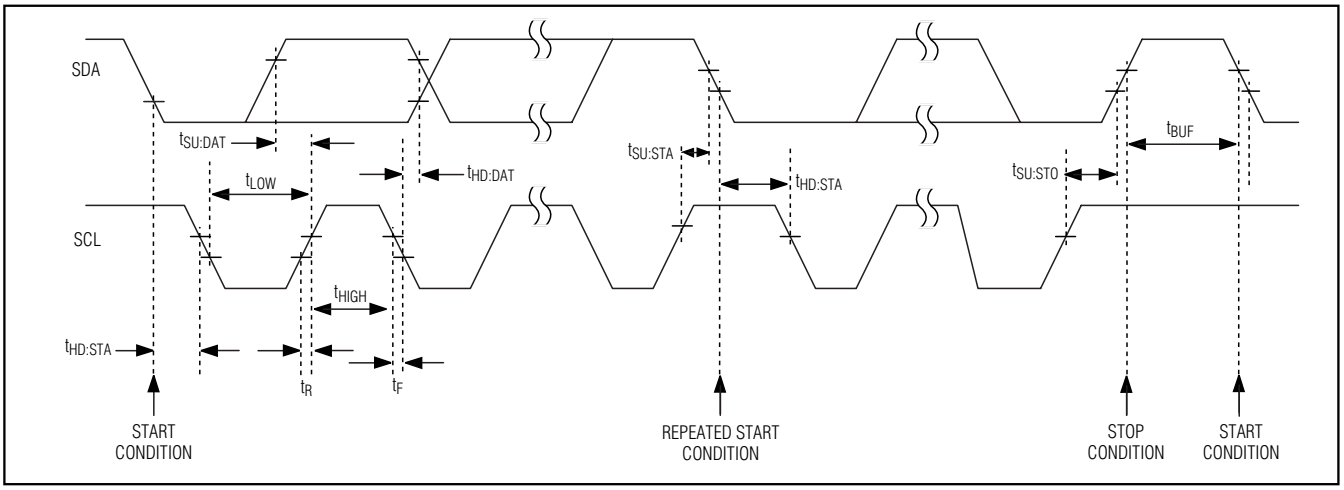

Figure 10. Serial-Interface Timing Details

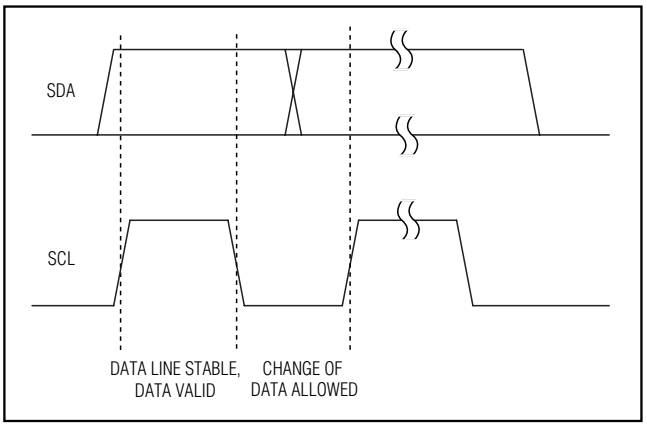

Figure 11. Bit Transfer

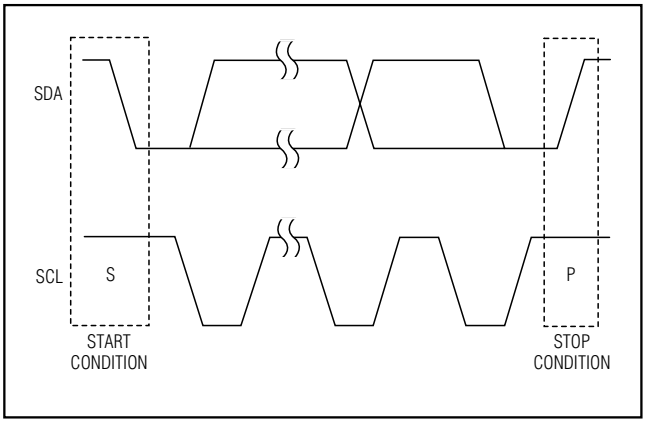

Figure 12. Start and Stop Conditions

Repeated START Conditions

A REPEATED START (SR) condition may indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation (see Figure 12). SR may also be used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX6876 serial interface supports continuous write operations with or without an SR condition separating them. Continuous read operations require SR conditions because of the change in direction of data flow.

Acknowledge

The acknowledge bit (ACK) is the 9th bit attached to any 8-bit data word. The receiving device always generates an ACK. The MAX6876 generates an ACK when receiving an address or data by pulling SDA low during the 9th clock period (Figure 13). When transmitting data, such as when the master device reads data back from the MAX6876, the device waits for the master device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if the receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time. The MAX6876 generates a NACK after the slave address during a software reboot, while writing to the EEPROM, or when receiving an illegal memory address.

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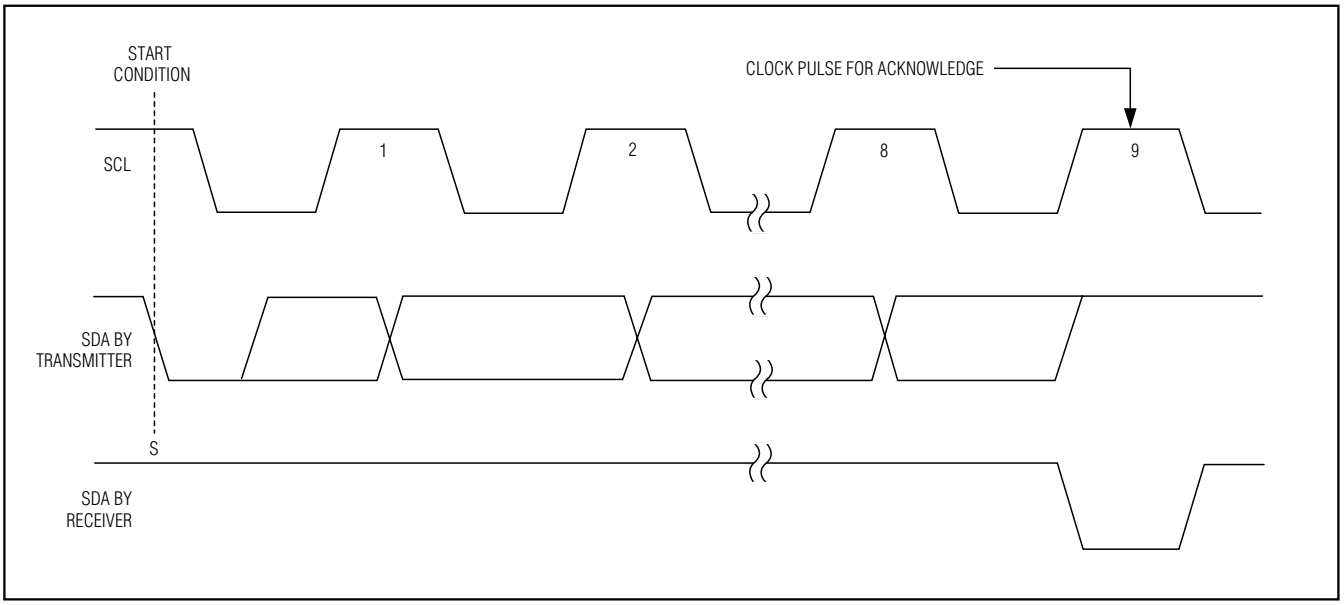

Figure 13. Acknowledge

Slave Address

The MAX6876 slave address conforms to the following table:

SA7 (MSB)	SA6	SA5	SA4	SA3	SA2	SA1	SA0 (LSB)
1	0	1	0	A1	A0	X	R/$\overline{W}$

X = *Don't care.*

SA7–SA4 represent the standard 2-wire interface address (1010) for devices with EEPROM. SA3 and SA2 correspond to the A1 and A0 address inputs of the MAX6876 (hardwired as logic low or logic high). SA0 is a read/write flag bit (0 = write, 1 = read).

The A0 and A1 address inputs allow up to four MAX6876s to connect to one bus. Connect A0 and A1 to GND or to HBP (see Figure 14).

Send Byte

The send byte protocol allows the master device to send one byte of data to the slave device (see Figure 15). The send byte presets a register pointer address for a subsequent read or write. The slave sends a NACK instead of an ACK if the master tries to send an address that is not allowed. If the master sends C0h or C1h, the data is ACK, because this could be the start of the write block or read block. If the master sends a stop condition, the internal address pointer does not change. If the master sends C4h, this signifies a software reboot. The send byte procedure follows:

1) The master sends a start condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit data byte.
5) The addressed slave asserts an ACK on SDA.
6) The master sends a stop condition.

Write Byte/Word

The write byte/word protocol allows the master device to write a single byte in the register bank, preset an EEPROM (configuration or user) address for a subsequent read, or to write a single byte to the configuration EEPROM (see Figure 15). The write byte/word procedure follows:

1) The master sends a start condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit command code.
5) The addressed slave asserts an ACK on SDA.
6) The master sends an 8-bit data byte.
7) The addressed slave asserts an ACK on SDA.

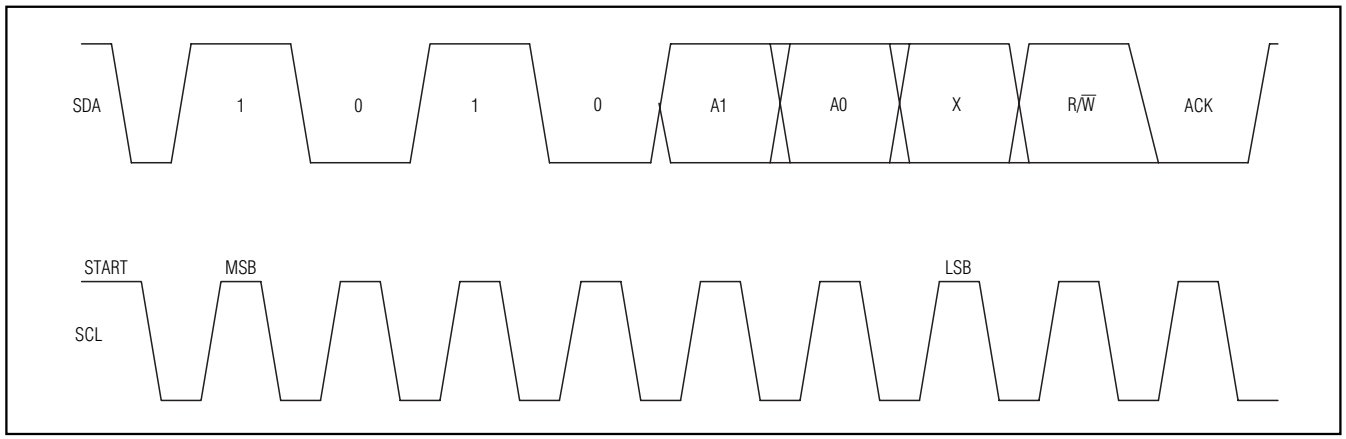

Figure 14. Slave Address

8) The master sends a stop condition or sends another 8-bit data byte.
9) The addressed slave asserts an ACK on SDA.
10) The master sends a stop condition.

To write a single byte to the register bank, only the 8-bit command code and a single 8-bit data byte are sent. The command code must be in the range of 00h to 13h to write on RAM or 20h to 33h to write on EEPROM. The data byte is written to the register bank if the command code is valid. The slave generates a NACK at step 5 if the command code is invalid.

Block Write

The block write protocol allows the master device to write a block of data (1 to 16 bytes) to the EEPROM or to the register bank (see Figure 15). The destination address must already be set by the send byte or write byte protocol. If the number of bytes to be written causes the address pointer to exceed 13h for the configuration register (or 33h for the configuration EEPROM), the address pointer stays at 13h (or 33h), overwriting this memory address with the remaining bytes of data. The last data byte sent is stored at register address 13h (or 33h). The block write procedure follows:

1) The master sends a start condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends the 8-bit command code for block write (83h).
5) The addressed slave asserts an ACK on SDA.
6) The master sends the 8-bit byte count (1 to 16 bytes), N.
7) The addressed slave asserts an ACK on SDA.
8) The master sends 8 bits of data.
9) The addressed slave asserts an ACK on SDA.
10) Repeat steps 8 and 9 N - 1 times.
11) The master generates a stop condition.

Block Read

The block read protocol allows the master device to read a block of 16 bytes from the EEPROM or register bank (see Figure 15). Read fewer than 16 bytes of data by issuing an early STOP condition from the master, or by generating a NACK with the master. The send byte or write byte protocol predetermines the destination address with a command code of C1h. The block read procedure follows:

1) The master sends a start condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends 8 bits of the block read command (C1h).
5) The slave asserts an ACK on SDA, unless busy.

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SEND BYTE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	DATA	ACK	P
	7 bits	0		8 bits		

Slave Address–equivalent to chip-select line of a 3-wire interface.

Data Byte–presets the internal address pointer.

WRITE WORD FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	DATA	ACK	DATA	ACK	P
	7 bits	0		8 bits		8 bits		8 bits		

Slave Address–equivalent to chip-select line of a 3-wire interface.

Write Address of the register you are writing to.

Data Byte–Data goes into the register set by the command.

Data Byte–Data goes into the next register set by the command.

WRITE BYTE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	DATA	ACK	P
	7 bits	0		8 bits		8 bits		

Slave Address–equivalent to chip-select line of a 3-wire interface.

Command Byte–selects register you are writing to.

Data Byte–data goes into the register set by the command.

BLOCK WRITE FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	BYTE COUNT= N	ACK	DATA BYTE 1	ACK	DATA BYTE ...	ACK	DATA BYTE N	ACK	P
	7 bits	0		8 bits		8 bits		8 bits		8 bits		8 bits		

Slave Address–equivalent to chip-select line of a 3-wire interface.

Command Byte–prepares device for block operation.

Data Byte–data goes into the register set by the command byte.

BLOCK READ FORMAT

S	ADDRESS	$\overline{WR}$	ACK	COMMAND	ACK	SR	ADDRESS	$\overline{WR}$	ACK	BYTE COUNT= 16	ACK	DATA BYTE 1	ACK	DATA BYTE ...	ACK	DATA BYTE N	ACK	P
	7 bits	0		8 bits			7 bits	0		10h		8 bits		8 bits		8 bits		

Slave Address–equivalent to chip-select line of a 3-wire interface.

Command Byte–prepares device for block operation.

Slave Address–equivalent to chip-select line of a 3-wire interface.

Data Byte–data goes into the register set by the command byte.

S = Start condition.
P = Stop condition.

Shaded = Slave transmission.
SR = Repeated start condition.

Figure 15. SMBus/I²C Protocols

Table 15. Configuration of Lock Bit

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
13h	33h	2	If 1, configuration registers are locked
			If 0, configuration registers unlocked

6) The master generates a repeated start condition.
7) The master sends the 7-bit slave address and a read bit (high).
8) The slave asserts an ACK on SDA.
9) The slave sends the 8-bit byte count (16).
10) The master asserts an ACK on SDA.
11) The slave sends 8 bits of data.
12) The master asserts an ACK on SDA.
13) Repeat steps 8 and 9 fifteen times.
14) The master generates a stop condition.

Address Pointers

Use the send byte protocol to set the register address pointers before read and write operations. For the configuration registers, valid address pointers range from 00h to 13h. Register addresses outside of this range result in a NACK being issued from the MAX6876. When using the block write protocol, the address pointer automatically increments after each data byte, except when the address pointer is already at 13h. If the address pointer is already 13h, and more data bytes are being sent, these subsequent bytes overwrite address 13h repeatedly, leaving only the last data byte sent stored at this register address.

For the configuration EEPROM, valid address pointers range from 20h to 33h. When using the block write protocol, the address pointer automatically increments after each data byte, except when the address pointer is already at 33h. If the address pointer is already 33h, and more data bytes are being sent, these subsequent bytes overwrite address 33h repeatedly, leaving only the last data byte sent stored at this register address.

Configuration EEPROM

The configuration EEPROM addresses range from 20h to 33h. Write data to the configuration EEPROM to automatically set up the MAX6876 upon power-up. Data transfers from the configuration EEPROM to the configuration registers when ABP exceeds UVLO during power-up. After ABP exceeds UVLO, an internal 1MHz clock starts after a 5µs delay, and data transfer begins. Data transfer disables access to the configuration registers and EEPROM. The data transfer from EEPROM to the configuration registers takes 2ms (max). Read configuration EEPROM data at any time after power-up or software reboot. Write commands to the configuration EEPROM are allowed at any time, unless the configuration lock bit is set (see Table 15). The maximum cycle time to write a single byte is 11ms (max).

Configuration Register Bank and EEPROM

The configuration registers can be directly modified with the serial interface without modifying the EEPROM, after the power-up procedure terminates and the configuration EEPROM data has been loaded into the configuration register bank. Use the write byte or block write protocols to write directly to the configuration registers. Changes to the configuration registers are lost upon power removal.

At device power-up, the register bank loads configuration data from the EEPROM. Configuration data can be directly altered in the register bank during application development, allowing maximum flexibility. Transfer the new configuration data byte-by-byte to the configuration EEPROM with the write byte protocol. The next device power-up or software reboot automatically loads the new configuration (Table 16).

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Table 16. Register Map

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/WRITE	DESCRIPTION
00h	20h	R/W	IN1 Undervoltage Threshold Value (V_{TH}): V_{TH} = 1.0 + n x 20mV (if R08[7] = 0) V_{TH} = 0.5 + n x 10mV (if R08[7] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
01h	21h	R/W	IN2 Undervoltage Threshold Value (V_{TH}): V_{TH} = 1.0 + n x 20mV (if R08[6] = 0) V_{TH} = 0.5 + n x 10mV (if R08[6] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
02h	22h	R/W	IN3 Undervoltage Threshold Value (V_{TH}): V_{TH} = 1.0 + n x 20mV (if R08[5] = 0) V_{TH} = 0.5 + n x 10mV (if R08[5] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
03h	23h	R/W	IN4 Undervoltage Threshold Value (V_{TH}): V_{TH} = 1.0 + n x 20mV (if R08[4] = 0) V_{TH} = 0.5 + n x 10mV (if R08[4] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
04h	24h	R/W	IN1 Overvoltage Threshold Value (V_{TH}): V_{TH} = 1.0 + n x 20mV (if R08[7] = 0) V_{TH} = 0.5 + n x 10mV (if R08[7] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
05h	25h	R/W	IN2 Overvoltage Threshold Value (V_{TH}): V_{TH} = 1.0 + n x 20mV (if R08[6] = 0) V_{TH} = 0.5 + n x 10mV (if R08[6] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
06h	26h	R/W	IN3 Overvoltage Threshold Value (V_{TH}): V_{TH} = 1.0 + n x 20mV (if R08[5] = 0) V_{TH} = 0.5 + n x 10mV (if R08[5] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.

Table 16. Register Map (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/WRITE	DESCRIPTION
07h	27h	R/W	IN4 Overvoltage Threshold Value (V_{TH}): V_{TH} = 1.0 + n x 20mV (if R08[4] = 0) V_{TH} = 0.5 + n x 10mV (if R08[4] = 1) where n is the register content decimal representation. Note that V_{TH} ranges must be 1V to 5.5V and 0.5V to 3.05V, respectively.
08h	28h	R/W	Bit 7—If 0, 20mV steps in V_{TH} setting for IN1 If 1, 10mV steps in V_{TH} setting for IN1
			Bit 6—If 0, 20mV steps in V_{TH} setting for IN2 If 1, 10mV steps in V_{TH} setting for IN2
			Bit 5—If 0, 20mV steps in V_{TH} setting for IN3 If 1, 10mV steps in V_{TH} setting for IN3
			Bit 4—If 0, 20mV steps in V_{TH} setting for IN4 If 1, 10mV steps in V_{TH} setting for IN4
			Bit 3—UV1 or OV1 Fault (read only for register address). If 1, IN1 is under undervoltage threshold or over overvoltage threshold. If 0, IN1 is over undervoltage threshold and under overvoltage threshold.
			Bit 2—UV2 or OV2 Fault (read only for register address). If 1, IN2 is under undervoltage threshold or over overvoltage threshold. If 0, IN2 is over undervoltage threshold and under overvoltage threshold.
			Bit 1—UV3 or OV3 Fault (read only for register address). If 1, IN3 is under undervoltage threshold or over overvoltage threshold. If 0, IN3 is over undervoltage threshold and under overvoltage threshold.
			Bit 0—UV4 or OV4 Fault (read only for register address). If 1, IN4 is under undervoltage threshold or over overvoltage threshold. If 0, IN4 is over undervoltage threshold and under overvoltage threshold.
09h	29h	R/W	Bit [7:6] If “00” the device configuration is a single device If “01” the device configuration is multiple devices, slave If “10” the device configuration is multiple devices, slave If “11” the device configuration is multiple devices, master
			Bit 5—If 1, latch-on fault If 0, autoretry
			Bit [4:2] “000” autoretry timer value = 25µs “001” autoretry timer value = 12.5ms “010” autoretry timer value = 25.0ms “011” autoretry timer value = 50.0ms “100” autoretry timer value = 100.0ms “101” autoretry timer value = 200.0ms “110” autoretry timer value = 400.0ms “111” autoretry timer value = 1600.0ms
			Bit 1—If 1, check I^2C enable bit If 0, ignore I^2C enable bit
			Bit 0—If 1 and 09h[1] = 1, I^2C enabled If 0 and 09h[1] = 1, I^2C disabled

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Table 16. Register Map (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/WRITE	DESCRIPTION
0Ah	2Ah	R/W	Bit [7:6] “00” fault power-up timer value = 25ms “01” fault power-up timer value = 50ms “10” fault power-up timer value = 100ms “11” fault power-up timer value = 200ms
			Bit [5:4] “00” fault power-down timer value = 25ms “01” fault power-down timer value = 50ms “10” fault power-down timer value = 100ms “11” fault power-down timer value = 200ms
			Bit 3—Reserved (write 0’s for EEPROM writes)
			Bit 2—Reserved (write 0’s for EEPROM writes)
			Bit 1—Reserved (write 0’s for EEPROM writes)
			Bit 0—Reserved (write 0’s for EEPROM writes)
0Bh	2Bh	R/W	Bit 7—If 1, OUT4 on ramp 2
			Bit 6—If 1, OUT3 on ramp 2
			Bit 5—If 1, OUT2 on ramp 2
			Bit 4—If 1, OUT1 on ramp 2
			Bit 3—If 1, OUT4 on ramp 1
			Bit 2—If 1, OUT3 on ramp 1
			Bit 1—If 1, OUT2 on ramp 1
			Bit 0—If 1, OUT1 on ramp 1
0Ch	2Ch	R/W	Bit 7—If 1, OUT4 on ramp 4
			Bit 6—If 1, OUT3 on ramp 4
			Bit 5—If 1, OUT2 on ramp 4
			Bit 4—If 1, OUT1 on ramp 4
			Bit 3—If 1, OUT4 on ramp 3
			Bit 2—If 1, OUT3 on ramp 3
			Bit 1—If 1, OUT2 on ramp 3
			Bit 0—If 1, OUT1 on ramp 3
0Dh	2Dh	R/W	Bit [7:6] “00” IN4 to OUT4 overcurrent threshold = 97.5% “01” IN4 to OUT4 overcurrent threshold = 95% “10” IN4 to OUT4 overcurrent threshold = 92.5% “11” IN4 to OUT4 overcurrent threshold = 90%
			Bit [5:4] “00” IN3 to OUT3 overcurrent threshold = 97.5% “01” IN3 to OUT3 overcurrent threshold = 95% “10” IN3 to OUT3 overcurrent threshold = 92.5% “11” IN3 to OUT3 overcurrent threshold = 90%
			Bit [3:2] “00” IN2 to OUT2 overcurrent threshold = 97.5% “01” IN2 to OUT2 overcurrent threshold = 95% “10” IN2 to OUT2 overcurrent threshold = 92.5% “11” IN2 to OUT2 overcurrent threshold = 90%
			Bit [1:0] “00” IN1 to OUT1 overcurrent threshold = 97.5% “01” IN1 to OUT1 overcurrent threshold = 95% “10” IN1 to OUT1 overcurrent threshold = 92.5% “11” IN1 to OUT1 overcurrent threshold = 90%

Table 16. Register Map (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/WRITE	DESCRIPTION
0Eh	2Eh	R/W	Bit [7:6] “00” overcurrent timer value = 12.5ms “01” overcurrent timer value = 50ms “10” overcurrent timer value = 100ms “11” overcurrent timer value = 200ms
			Bit 5—If 1, overcurrent monitoring on OUT1 is enabled If 0, no overcurrent monitoring on OUT1
			Bit 4—If 1, overcurrent monitoring on OUT2 is enabled If 0, no overcurrent monitoring on OUT2
			Bit 3—If 1, overcurrent monitoring on OUT3 is enabled If 0, no overcurrent monitoring on OUT3
			Bit 2—If 1, overcurrent monitoring on OUT4 is enabled If 0, no overcurrent monitoring on OUT4
			Bit [1:0] Not used
0Fh	2Fh	R/W	Bit [7:5] “000” gate1-delay timer value = 25µs “001” gate1-delay timer value = 12.5ms “010” gate1-delay timer value = 25.0ms “011” gate1-delay timer value = 50.0ms “100” gate1-delay timer value = 100.0ms “101” gate1-delay timer value = 200.0ms “110” gate1-delay timer value = 400.0ms “111” gate1-delay timer value = 1600.0ms
			Bit 4—Not used
			Bit 3—OC1 overcurrent fault (read only for register address). If 1, OC1 is overcurrent. If 0, OC1 is not overcurrent.
			Bit 2—OC2 overcurrent fault (read only for register address). If 1, OC2 is overcurrent. If 0, OC2 is not overcurrent.
			Bit 1—OC3 overcurrent fault (read only for register address). If 1, OC3 is overcurrent. If 0, OC3 is not overcurrent.
			Bit 0—OC4 overcurrent fault (read only for register address). If 1, OC4 is overcurrent. If 0, OC4 is not overcurrent.
10h	30h	R/W	Bit [7:6] “00” IN4 to OUT4 power-good threshold = 95% “01” IN4 to OUT4 power-good threshold = 92.5% “10” IN4 to OUT4 power-good threshold = 90% “11” IN4 to OUT4 power-good threshold = 87.5%
			Bit [5:4] “00” IN3 to OUT3 power-good threshold = 95% “01” IN3 to OUT3 power-good threshold = 92.5% “10” IN3 to OUT3 power-good threshold = 90% “11” IN3 to OUT3 power-good threshold = 87.5%
			Bit [3:2] “00” IN2 to OUT2 power-good threshold = 95% “01” IN2 to OUT2 power-good threshold = 92.5% “10” IN2 to OUT2 power-good threshold = 90% “11” IN2 to OUT2 power-good threshold = 87.5%
			Bit [1:0] “00” IN1 to OUT1 power-good threshold = 95% “01” IN1 to OUT1 power-good threshold = 92.5% “10” IN1 to OUT1 power-good threshold = 90% “11” IN1 to OUT1 power-good threshold = 87.5%

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Table 16. Register Map (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/WRITE	DESCRIPTION
11h	31h	R/W	Bit 7—If 1, OUT1 also controls $\overline{\text{RESET}}$ If 0, OUT1 does not control $\overline{\text{RESET}}$
			Bit 6—If 1, OUT2 also controls $\overline{\text{RESET}}$ If 0, OUT2 does not control $\overline{\text{RESET}}$
			Bit 5—If 1, OUT3 also controls $\overline{\text{RESET}}$ If 0, OUT3 does not control $\overline{\text{RESET}}$
			Bit 4—If 1, OUT4 also controls $\overline{\text{RESET}}$ If 0, OUT4 does not control $\overline{\text{RESET}}$
			Bit [3:1] “000” reset timer value = 25µs “001” reset timer value = 12.5ms “010” reset timer value = 25.0ms “011” reset timer value = 50.0ms “100” reset timer value = 100.0ms “101” reset timer value = 200.0ms “110” reset timer value = 400.0ms “111” reset timer value = 1600.0ms
			Bit 0. If 1, selects external reference, if 0 internal reference selected
12h	32h	R/W	Bit [7:6] “00” track/sequence slew rate (rise or fall) = 800V/s “01” track/sequence slew rate (rise or fall) = 400V/s “10” track/sequence slew rate (rise or fall) = 200V/s “11” track/sequence slew rate (rise or fall) = 100V/s
			Bit [5:3] Not used
			Bit 2—Reserved (write 0’s for EEPROM writes)
			Bit 1—Reserved (write 0’s for EEPROM writes)
			Bit 0—Reserved (write 0’s for EEPROM writes)
13h	33h	R/W	Bit 7—If 1, reverse order of track/sequence power-down If 0, GATE_ fast pulldown
			Bit 6—If 1, OUT1 pulldown with 100Ω If 0, OUT1 100Ω pulldown disabled
			Bit 5—If 1, it is possible to discharge OUT2 with a pulldown If 0, no pulldown is allowed
			Bit 4—If 1, it is possible to discharge OUT3 with a pulldown If 0, no pulldown is allowed
			Bit 3—If 1, it is possible to discharge OUT4 with a pulldown If 0, no pulldown is allowed
			Bit 2—If 1, configuration registers are locked If 0, configuration registers unlocked
			Bit [1:0] not used
14h	34h	—	Reserved. Should not be overwritten.
15h	35h	—	Reserved. Should not be overwritten.
16h	36h	—	Reserved. Should not be overwritten.

Table 16. Register Map (continued)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	READ/WRITE	DESCRIPTION
17h	37h	—	Reserved. Should not be overwritten.
18h	38h	—	Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
19h	39h	—	Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
1Ah	3Ah	—	Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
1Bh	3Bh	—	Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
1Ch	3Ch	—	Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
1Dh	3Dh	—	Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
1Eh	3Eh	—	Reserved. Should not be overwritten.
1Fh	3Fh	—	Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.
			Reserved. Should not be overwritten.

Applications Information

Layout and Bypassing

For better noise immunity, bypass each of the voltage-detector inputs to GND with 0.1µF capacitors installed as close to the device as possible. Bypass ABP to GND with 1µF capacitors installed as close to the device as possible. ABP is an internally generated voltage and should not be used to supply power to external circuitry.

Configuration Latency Period

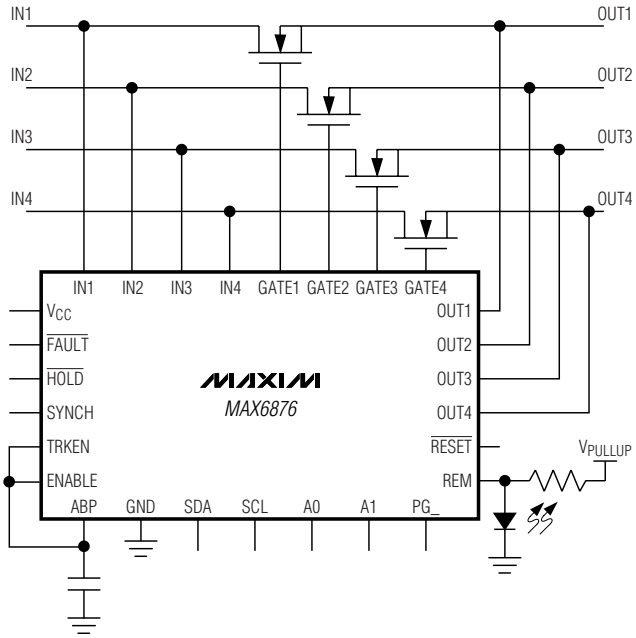
A delay of less than 5µs occurs between writing to the configuration registers and the time when these changes actually take place, unless when changing one of the voltage detector's thresholds. Changing a voltage-detector threshold typically takes 150µs. When changing EEPROM contents, software reboot or cycling of power is required for these changes to transfer to volatile memory.

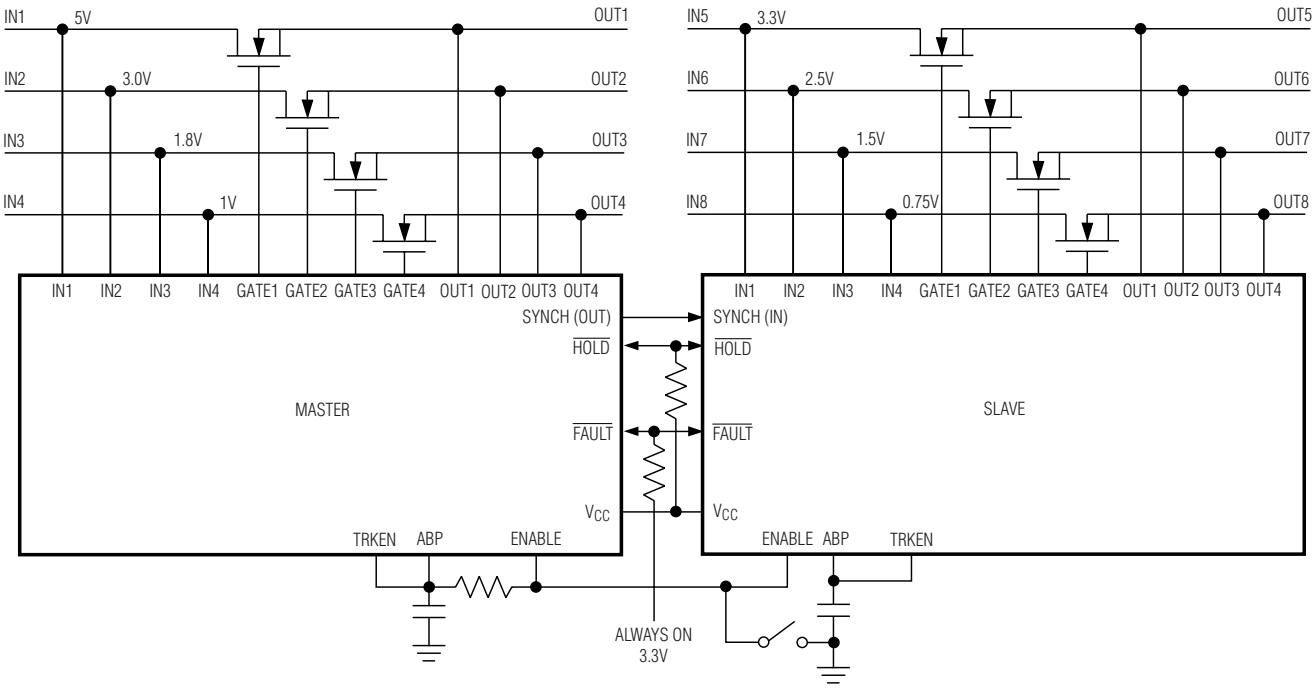
Chip Information

PROCESS: BiCMOS

EEPROM-Programmable, Quad, Power-Supply Tracker/Sequencer Circuit

Typical Application Circuits



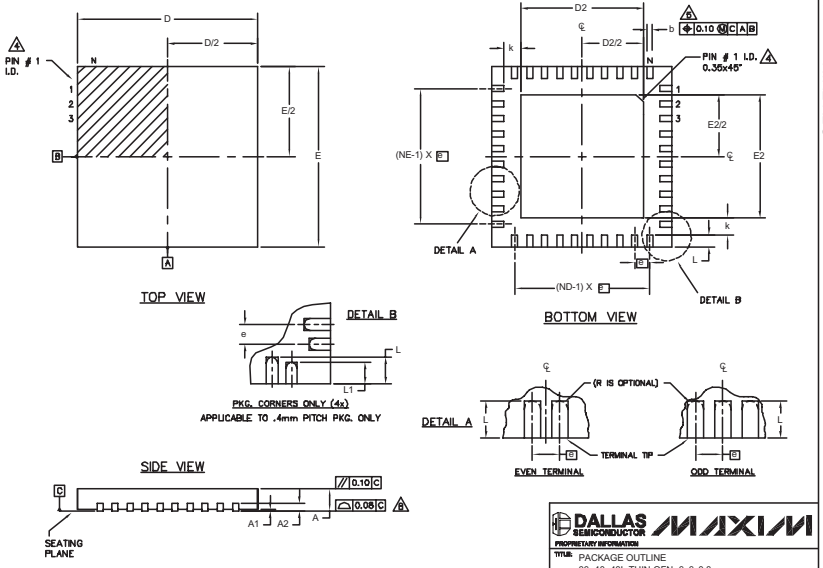


NOTE: CONFIGURING THE MAX6876 FOR MASTER/SLAVE OPERATION.

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN 6x6x0.8.EPS



COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	–	–	–	–	–	–	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS							DOWN BONDS ALLOWED
PKG. CODES	D2			E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 36, 40, 48L THIN QFN, 6x6x0.8mm
DOCUMENT CONTROL NO. 21-0141
REV. E
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